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CMOS LOGIC FAMILIES FOR VLSI DESIGN

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ABSTRACT

In this paper, the investigation and evaluation of different stateof-the-art CMOS logic families, currently in use for VLSI design, are performed. These logic families are static CMOS logic, Pseudo-NMOS logic, Domino logic and Two-phase dynamic logic (TPDL). The main characteristics of these logic families, which are, power consumption, layout area and ease of implementation, are analyzed and compared.

For the comparison among the different logic families, three basic logic gates are implemented using each of these logic families. The implemented gates are an Inverter, a 2-input NAND, and a 2-input NOR gates. The simulation is performed using Tanner-Pro tools for different technologies starting from 1.6 um to 0.25 um feature size at a power supply voltage (Vdd) of 5 volts. The technology parameters were extracted and measured from a fabrication lot by MOSIS SCN16 to SCN025.

KEYWORDS

- VLSI design.
- Logic families.
- Static CMOS.
- Pseudo–NMOS.
- Domino logic.
- TPDL.

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1. INTRODUCTION

Digital VLSI circuit designers always search for logic circuit designs that provide maximum performance with minimum power consumption and layout area. Here, we conduct a comparative study of the above-mentioned parameters for both static and dynamic CMOS logic families used in VLSI design. The studied static logic families are Static CMOS logic and Pseudo-NMOS logic. The choice of these two families is due to their popularity in the advanced electronic design automation (EDA) area. Most of the EDA tools have their library modules designed in static methodology. They are designed this way due to their ease and straightforward VLSI implementation techniques. The studied dynamic logic families are Domino and (TPDL) logic. The choice of these two families is due to their popularity and efficiency among all dynamic logic families.

2. DESIGN METHODOLOGY

2.1. Static CMOS Logic:

The principle of operation of static CMOS logic is to pull down the output to ground through an N–Logic block and pull it up to Vdd through a P-Logic block. Figure (1.a) shows the circuit diagram of a static CMOS Inverter. When the input is logic "low", the PMOS transistor is "ON" and the output is charged to Vdd, while the NMOS transistor is "off". When the input is logic "high", the PMOS transistor is "OFF", and the NMOS transistor is "ON". In this case, the output is discharged to ground. When the input is not switching, the output is either low or high. In this case, one of the transistors is "off" while the other is "ON", thus preventing any currentto flow from Vdd to ground except for the leakage currents. This reduces the power consumption, which is the basic advantage of fabricating both N- and P- transistor on the same die.

During switching, when both transistors are in saturation region there is a short circuit current. This occurs when both NMOS and PMOS devices are "ON" for a short time thus sinking a lot of current from Vdd to ground. Therefore, the power consumption will increase with the increase of the switching frequency.

The "hole" mobility (u_p) for silicon equals 1/3 to 1/2 its electron mobility (u_n) so, the use of the slower PMOS device for output evaluation limits the maximum operating frequency of the designed circuit. To have equal rise and fall times for the inverter of Fig. (1.a), a PMOS transistor that is 2 to 3 times wider than the NMOS transistor is used.

Figure (2.a) shows a 2-Input static "NAND" gate that uses four transistors. Implementing N-input static CMOS gate needs 2N transistors. In the 2-Input NAND, two NMOS transistors are connected in series, which is equivalent to one transistor of double length. The discharging time through the long NMOS will take two times longer to discharge the output to ground (W/L ratio is decreased due to doubling of its L) This doubles the fall time of the output waveform. Similarly, Fig. (3.a) shows a 2-Input static "NOR" gate in which 2 PMOS transistors are connected in series. This is equivalent to one longer transistor, which doubles the "already long" rise time. This enhances the main disadvantage of static CMOS logic gates. Widening the PMOS transistor will solve part of this problem at the expense of increased power consumption and layout area [1].

Having a wide PMOS increases W/L ratio of the transistor but in the mean time will increase the MOS capacitance, which will again increase the delay of the circuit.

2.2. Pseudo-NMOS Logic:
Pseudo-NMOS logic uses only one PMOS device as a pull-up device for a multi-transistor N-Logic block. Therefore, the required number of transistors for an N-input gate is an N+1 transistor. The used PMOS device has its gate connected to ground and is therefore always "ON". When the N-Logic block is "OFF", the output is charged to Vdd. When the N-block is "ON", a large current can pass from Vdd to ground, causing large power consumption, whenever the N-block is "ON". Device dimensions, for Pseudo-NMOS, must be carefully chosen in order to allow the output to be discharged to ground. The PMOS device must be chosen wide enough to conduct a multiple of the N-block's leakage current when the output is "high", and narrow enough so that the N-block can still pull down the output safely. Therefore, Pseudo-NMOS logic is a ratioed logic. The circuit diagram of a Pseudo-NMOS inverter, NAND and NOR gates is shown in Fig.(1.b), Fig(2.b) and Fig.(3.b) respectively.
Pseudo-NMOS logic has the advantage of higher speed than static CMOS logic; especially in large fan-in NOR gates. This is due to the fact that there is only one PMOS transistor contributing for the output rise time. The overall speed improvement is substantial, at the cost of a slight increase in power consumption.

2.3. Basic Dynamic Logic:
Dynamic logic circuits use two clocked NMOS and PMOS devices in addition to the main N-logic block, as shown in Fig. (4.a). Dynamic logic relies on the storage of signal voltages on parasitic capacitances at certain circuit nodes. Because charge will leak with time, the circuits need to be periodically refreshed, and thus the presence of a clock with a certain specified minimum frequency is essential [2]. The output of the N-logic block is pre-charged to Vdd through the clocked PMOS transistor, and is conditionally discharged to ground through the clocked NMOS transistor. The use of clocked transistors prevents direct current flow from Vdd to ground that occurs in both static CMOS and Pseudo-NMOS logic families. This largely reduces the dynamic power consumption.
Dynamic logic has two-phases of operation, a pre-charge phase and an evaluation phase. In the pre-charge phase (Clock "low"), the output node is charged to Vdd regardless of input logic levels. Inputs can change only during this phase. At the completion of the pre-charge phase, the path to Vdd is turned "OFF" while the path to ground is conditionally turned "ON" by the clocked NMOS device (Clock "high"). During the evaluation phase, the pre-charged output node either remains high or is pulled down according to the input logic levels. Since in each phase either the path to Vdd or to ground is active, the logic levels are not determined by the width and length ratios of the load and clocked transistors. Therefore, dynamic logic is a non-ratioed logic.
The main drawback of dynamic logic is the need to route the clock signal to every gate in the circuit, which aggravates the routing problem and increases the parasitic capacitances. Another drawback is the need for refreshing with a minimum clock frequency for correct circuit operation.

A strong limitation of the basic dynamic logic structure that uses only one clock, is the impossibility of cascading the logic blocks to implement a complex logic function. Figure (4.b) shows two cascaded single-input dynamic logic gates. In this case, by the end of the pre-charge phase, nodes (N1) and (N2) are charged to Vdd. During the evaluation phase, if input A is high, the output of the first gate, (N1), will start to discharge. Due to the finite discharge time of CL1, the pre-charged node (N1) will discharge the output node of the following gate (N2) before the output of the first stage (N1) is correctly evaluated (i.e. before CL1 is completely discharged). This causes an error logic level for node (N2) as shown in the timing diagram in fig (4.c). Thus, the basic dynamic logic blocks can not be cascaded together to perform a more complex function.

2.4. Domino Logic:

Domino logic modifies the basic dynamic structure by adding a static inverter to each logic gate output. This allows a single clock to pre-charge and evaluate a cascaded set of dynamic domino logic blocks without having error logic levels, (which occurs in the simple dynamic logic). Figure (5.a) shows two cascaded single-input domino logic gates. The pre-charge phase can be described as follows:

A logic "low" on the CLK input starts the pre-charge phase.

- -Node X1 will be charged "high" through Mp1 and CL1.
- -Node Y1 will be "low" after a certain delay.
- -Node X2 will be charged "high" through Mp2 and CL2.
- -Node Y2 will be "low" after a certain delay.

A logic "high" on the CLK input ends the pre-charge phase and starts the evaluation phase. Assuming input A is high at the beginning of evaluation, CL1 will begin discharging, pulling X1 down. Meanwhile, the low level at Y1 keeps M2 OFF, and CL2 remains fully charged until X1 falls below the threshold voltage of inverter I1, causing Y1 to go up. When Y1 goes up, it turns M2 ON, causing CL2 to begin to discharge, pulling X2 low and Y2 high. Obviously, this solves the problem of the basic dynamic circuit described earlier.

As shown in fig (5.b), output Y1 will make a 0-to-1 transition t_{PLH} seconds after the rising edge of the clock. Subsequently, Y2 makes a 0-to-1 transition after another t_{PLH} interval. The propagation of the rising edge through a cascade of gates thus resembles dominoes falling over in a cascade manner [2]. Domino CMOS logic finds application in the design of address decoders in memory chips [2].

The above description shows that during the precharge phase, the output of the first dynamic gate is high and the inverter output is low. Thus the transistors (or generally the N-logic blocks) they drive are OFF. During the evaluation phase, the domino logic gate output can only make a transition from low to high. Consequently, there will be no switching hazards at any node in the circuit because nodes can make at most a single transition and then must remain stable until the next pre-charge phase. In a cascaded set of logic blocks, each stage evaluates and then causes the next stage to evaluate. That is why this domino structure is sometimes called "Buffered Domino". The design of a Domino Inverter, NAND and NOR gates are shown in fig. (1.c), fig. (2.c) and fig. (3.c) respectively.

Dynamic domino logic gates have low power consumption because there is no direct path of current from Vdd to ground except for the static inverter. Since indomino logic an input signal has to drive only 1 NMOS gate, the load capacitances at the inputs are much smaller compared to those of static gates. In addition, using a single clock in domino circuits provides a simple operation and full utilization of the speed of each gate [3].
The main limitation of this dynamic technique is that all of the gates are non-inverting, meaning that it does not form a complete logic family. Another limitation is that a static inverter must buffer each gate, meaning that this technique is not completely dynamic [4].

2.5. Two-Phase Dynamic Logic (TPDL)
As shown in Fig (6), this family uses only NMOS transistors in evaluating the output. As the first stage evaluates its output node (N1), the second stage will be precharging and vise versa. The two successive blocks are fed from two non-overlapping clock phases. A pass gate is used between successive logic blocks to isolate the data stored at the input of the second block from corruption when the output of the first block is precharging. The two clock phases CLK1 and CLK2 are non-overlapped in the logic low level. The main disadvantage of this family is the use of extra metallization to run the two clock phases and their complements [5,6].
PMOS transistors are used only for prechaging the output nodes. Also, there is no direct current path from supply voltage to ground at any time, which eliminates static and short-circuit power consumption in this logic family. The evaluating transistor block NMOS can be designed using minimum size transistors (in most cases) without affecting the noise margins or the speed. This will reduce both the layout area and the consumed power. Increasing the sizes of the evaluating transistor block will increase the drive capability of the circuit, but wil increase the output capacitance which decreases the maximum operating frequency (trade off). As the number of transistors in the evaluating transistor block increases, the size of the clocked PMOS needs to be increased to be able to quickly charge the output node [7].
The detailed operation of the circuit is as follows. When CLK1 is low and CLK2 is high, the CLK1 stage is precharging its output node N1 through the ON transistor Ql. At the same time, the input data is passed to the N-logic block through the ON CLK1 pass gates. The precharged output of this stage is isolated from the inputs of the next CLK2 stage by the next OFF CLK2 pass gate. The CLK2 stage is evaluating the data stored on the N-logic block inputs (CLK2 is high and Q3 is OFF while Q4 is ON). The evaluated output is passed to the next CLK1 stage through the ON CLK1 pass gate. When CLK1 is high and CLK2 is low, the CLK2 stage is evaluating the data stored on the input of the N-logic block. The output (node N1) is fed to the next CLK2 stage through the ON CLK2 pass gate. At the same time, the CLK2 stage is precharging the output which is isolated from the next CLK1 stage by the OFF CLK1 pass gate. When both CLK1 and CLK2 are high at the same time (they are non-overlapped in the logic low), both stages (CLK1 and CLK2) will be evaluating the inputs stored on the N-logic blocks. The outputs of both stages will be isolated from the next stage by the OFF pass gates so there is no corruption of data. The two phases must be non-overlapped in the low state to prevent data corruption. If this condition is not satisfied and both phases are low at the same

time, both stages will precharge their output nodes and the precharged outputs will be passed to the inputs of the next stage. When either CLK1 or CLK2 switches to logic low, the corresponding stage will start to evaluate the erroneous inputs (precharged outputs of the previous stages) and give an erroneous output. If any input to a CLK1 stage is supplied from another circuit (non-TPDL circuit), it has to be stable (unchanging) during CLK1 logic low. Similarly, if any input to a CLK2 stage is supplied from a non-TPDL circuit, this input has to be stable during CLK2 logic low. Another condition that must be satisfied is that CLK1 stage outputs can only be connected to CLK2 stage inputs and CLK2 stage outputs can only be connected to CLK1 stage inputs [6]. The TPDL inverter, NAND and NOR gates are shown in fig. (1.d), fig. (2.d) and fig. (3.d) respectively.

3. COMPARISON AMONG THE DIFFERENT LOGIC FAMILIES:

3.1. Static CMOS advantages:

- Easy to design and to translate logic function to transistors (for N Inputs we need 2N transistors).
- Good noise margins (frequency dependent).
- Low static power consumption since transistors are OFF (only dynamic power during switching).
- Transistor sizing is not a critical issue for correct circuit operation.

Static CMOS disadvantages:

- Increased layout area (for N inputs we need 2N transistors).
- Heavy loading of inputs (Every input has to drive 1NMOS gate and1PMOS).
- PMOS width should be at least twice the NMOS width to get an equal high and low noise margins (electron mobility is about twice the hole mobility).
- Transistors connected in Series reduce speed especially PMOS transistors.

3.2. Pseudo-NMOS advantages:

- Easy to translate logic to transistors (for N inputs we need N+1 transistors).
- Decreased layout area (for N inputs we need N+1 transistors).
- Lower loading of inputs (Every input has to drive only 1 NMOS gate).
- PMOS is not used for output level evaluation.

Pseudo-NMOS disadvantages:

- Transistor sizing is critical for correct circuit operation.
- Dissipate static power whenever output is low.
- Reduced logic levels hence lower noise immunity.

3.3. Domino logic advantages:

- Only fast NMOS transistors are used for output evaluation
- Low static power consumption
- Non ratioed logic
- Decreased layout area
- Increased operating frequency

Domino logic disadvantages:

- Complex to design

- Not a complete logic family
- Routing problems for the clock signal.

3.4. TPDL logic advantages:

- Only fast NMOS transistors are used for output evaluation
- The lowest power consumption.
- Highest operating frequency.
- Reduced layout area.
- Good Noise margin
- Constitute a complete logic family
- No need for a static inverter
- Non ratioed logic

TPDL logic disadvantages:

- Design Complexity
- Uses two clocks and their complement (routing complexity)
- Need on chip clock generator.

4. SIMULATION RESULTS

In this paper, the design, analysis and implementation of different experimental CMOS dynamic logic circuits have been documented. Dynamic logic circuits offer several advantages over typical static logic circuits. They have a higher speed and lower power consumption than static logic. The non-ratioed nature of dynamic logic reduces its layout area.

The maximum operating frequency of the implemented circuits in static logic is 800 MHz. Domino dynamic logic circuits have the smallest layout area. The use of a static inverter in Domino logic gates increases its power consumption. Also, only noninverting functions can be implemented using Domino logic. The maximum operating frequency of the designed Domino logic circuits is 1.2 GHz.

TPDL uses only the fast N-channel transistors in evaluating the logic function. The slow P-channel transistors are used only to precharge the output nodes. Because of the pass gates in front of each evaluating circuit, TPDL designs are selflatching and are suitable for pipelined architectures. Therefore, any circuit can be pipelined to reach the maximum frequency of operation without adding any storage elements (pipeline registers). The maximum frequency of the designed TPDL logic circuits is 1.6 GHz.

The basic combinational logic gates (Inverter, NAND gate, NOR gate) are designed and implemented in TPDL and static logic. These gates are used in the design and the fabrication of more complex circuits. TPDL gates have a maximum operating frequency of 1.6 GHz, while the static logic gates operate up to 0.8 GHz The power consumption of TPDL gates is less than one-half that of the static logic gates when powered from the same power supply and having the same fan-out.

The comparison in performance among all the studied dynamic and static logic families is completed through the implemented circuits. Figure (7) shows the comparison among the Static, Pseudo-NMOS, Domino and TPDL Inverters in their power consumption and maximum operating frequency. While fig. (8) shows the same comparison among the

Static, Pseudo-NMOS, Domino and TPDL NAND gate. Finally, fig (9) shows the same comparison among the Static, Pseudo-NMOS, Domino and TPDL NOR gate. TPDL circuits have the highest maximum operating frequency and the lowest power consumption.
In addition, the layout area will be about half that of the static logic circuit and about the same as that of the Domino logic circuits. The power consumption of the TPDL circuits is less than one-half that of the static logic circuits. TPDL power consumption is comparable to that of the Domino circuit at low frequency (up to 800 MHz), and about two third of the Domino beyond this frequency. The main disadvantage of the TPDL design is that it requires two non-overlapped clock phases and their complements for proper operation. In addition, routing these four clock phases to all of the circuit increases the design complexity.

5. CONCLUSION

The results presented in this paper show that CMOS TPDL circuits have about double the operating frequency of static logic circuits performing the same function. Also, they dissipate less than one-half the power consumption compared to static logic when powered from the same supply voltage. CMOS TPDL circuits have the lowest power consumption among the studied dynamic logic families. It also have the lowest delay power product ever reported. CMOS TPDL circuits are the most complex design and contain many traps for the beginner designer. TPDL is an excellent candidate logic family for the next generation of high speed, high density and low power processors

6. REFERENCES

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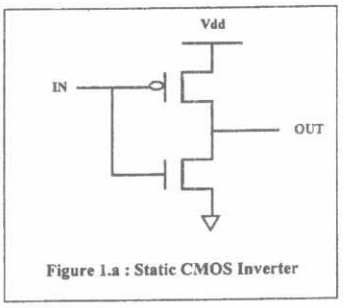

Figure 1.a : Static CMOS Inverter

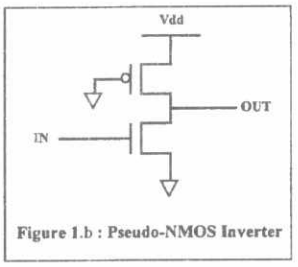

Figure 1.b : Pseudo-NMOS Inverter

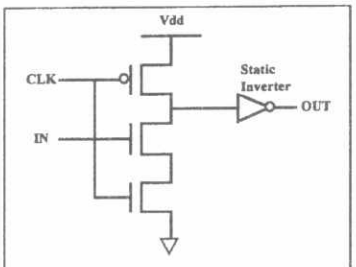

Figure 1.c : Domino Inverter Logic Gate

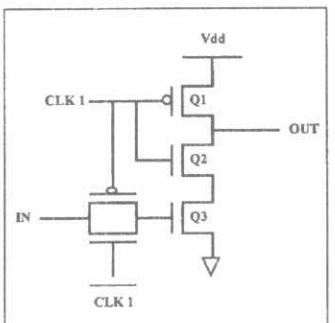

Figure 1.d : TPDL Inveter

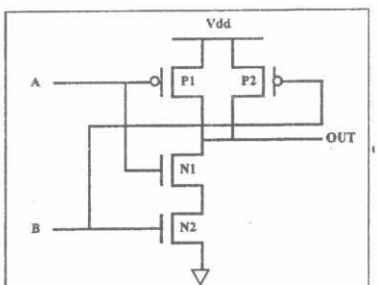

Figure 2.a : 2-Input Static NAND Gate

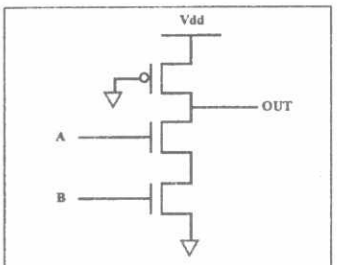

Figure 2.b : Pseudo-NMOS NAND Gate

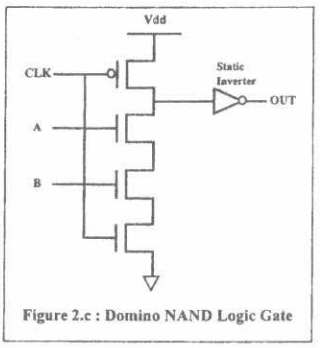

Figure 2.c : Domino NAND Logic Gate

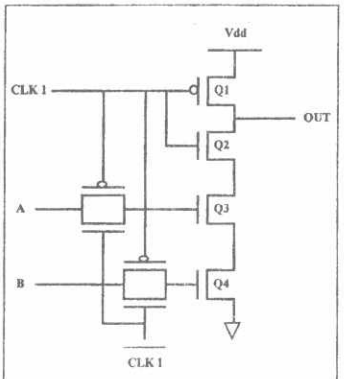

Figure 2.d : TPDL NAND Gate

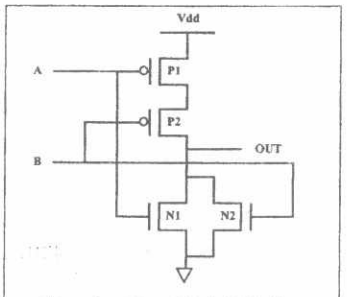

Figure 3.a : 2-Input Static NOR Gate

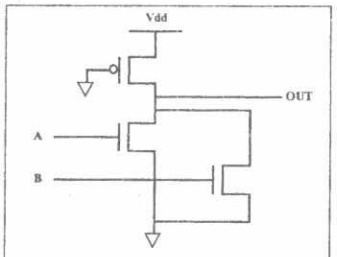

Figure 3.b : Pseudo-NMOS NOR Gate

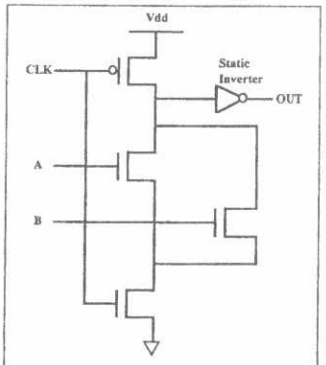

Figure 3.c : Domino NOR Logic Gate

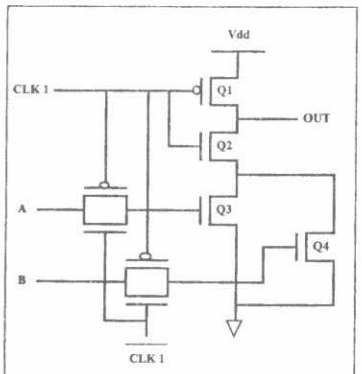

Figure 3.d : TPDL NOR Gate

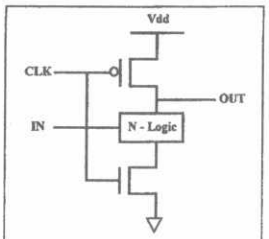

Figure 4.a : Simple Dynamic Logic Gate

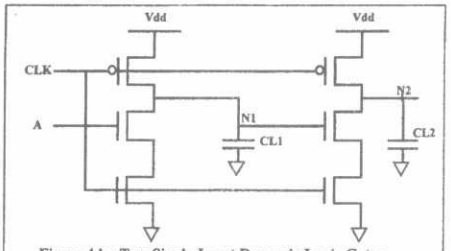

Figure 4.b : Two Single-Input Dynamic Logic Gates Connected in Cascade

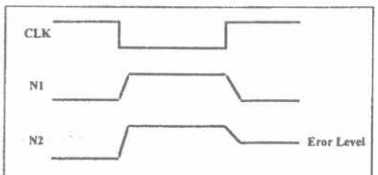

Figure 4.c : Erroneous Evaluation in Cascaded Dynamic Logic Gates

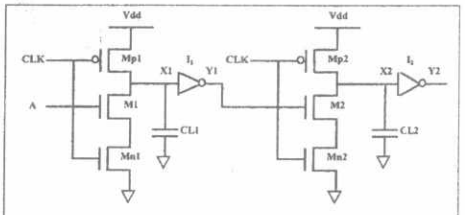

Figure 5.a : Two Cascaded Single-Input Domino Logic Gates

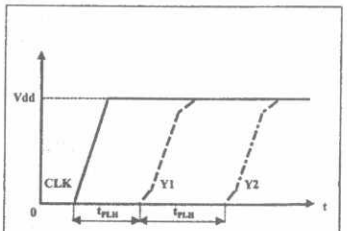

Figure 5.b : Waveforms of Two Cascaded Single Input Domino Logic Gates During the Evaluation Phase

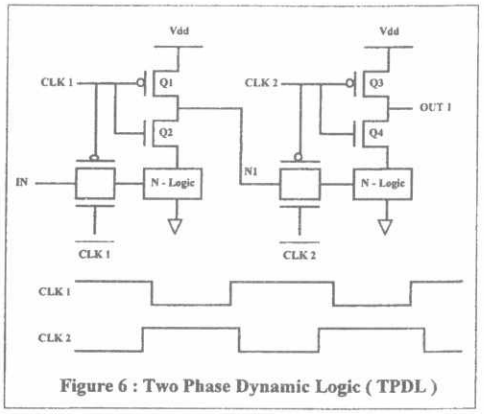

Figure 6 : Two Phase Dynamic Logic (TPDL)

Freq. (Hz)		2M	20M	200M	400M	800M	1200M	1600M
Power (uW)	*Pseudo*	3404	3761.77	4687.33	5041.48	5495.4		
	Static	54.56	402.59	821.48	1079.94	1593.33		
	Domino	3.19	40.45	318.07	623.66	863.51	3917.9	
	TPDL	1.72	28.65	168.9	552.07	806.48	3131.71	2849.93

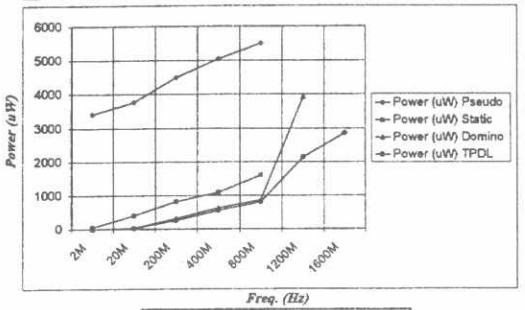

Figure 7 : Inverter (Tech. = 0.25u)

Freq. (Hz)		2M	20M	200M	400M	800M	1200M	1600M
Power (uW)	*Pseudo*	1346.25	1687.21	2314.21	2593.04	2918.1		
	Static	59.92	438.22	747.01	806.85	949.69		
	Domino	2.8	37.61	368.16	691.83	827.3	4313.85	
	TPDL	1.54	15.19	146.34	638.81	816.47	1750.31	3350.68

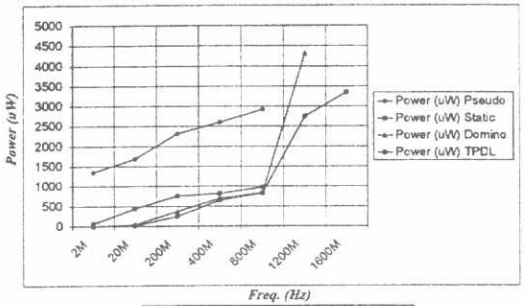

Figure 8 : NAND (Tech. = 0.25u)

Freq. (Hz)		2M	20M	200M	400M	800M	1200M	1600M
Power (uW)	*Pseudo*	2687.97	3034.86	3467.04	3608.22	3637.02		
	Static	55.54	191.94	490.06	589.6	642.56		
	Domino	4.35	42.82	433.28	548.58	632.75	3887.43	
	TPDL	2.05	19.69	333.1	482.07	590.48	3344.05	5404.06

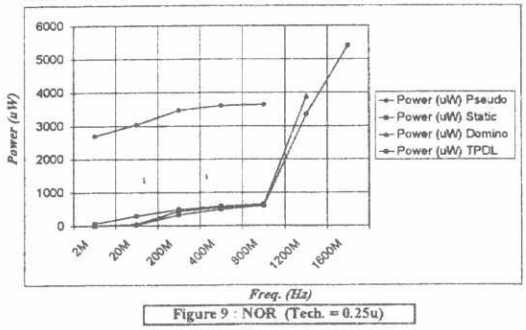

Figure 9 : NOR (Tech. = 0.25u)