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EFFICIENT FPGA ARCHITECTURE OF GREY-SCALE SOFT MORPHOLOGICAL FILTERS FOR IMAGE AND VIDEO RESTORATION

Hamid* M. S. and Ragab* A. S.

Recently, Soft Morphological Filters have shown excellent performance in restoring noisy images. To add soft morphological filters in image processing chains and also to process image sequences in real time, it became a necessity to implement soft morphological operations in hardware. In this paper, FPGA architecture of grey-scale soft morphological filters is proposed. The architecture is based on a stack filter expression with some modification. The design can calculate soft morphological operations of greyscale soft morphological filters with structuring functions of any size and shape inside the structuring function's overall support. The filter architecture guarantees fixed processing time independent of the size and shape of the structuring function of the filter. Implementation results showed that the proposed filter architecture is suitable for real time applications.

Key Words: FPGA, Soft Morphological Filters, and Image Restoration

* Egyptian Armed Forces

I. INTRODUCTION

Implementation of signal and image processing applications on VLSI devices became of increasing interest in recent years with the increased transfer of signal and image data on communication networks such as the internet, mobile phone networks, switched data networks, and satellite links. Some of these applications include video coding [1], video-object segmentation [2], image restoration using nonlinear filters [3, 4, 5], medical imaging [6], signal and image processors [7, 8], and real-time image enhancement [9]. Hence, this requires the realization of many signal and image processing architectures on hardware chips such that they can be integrated with digital multimedia systems.

Because of their parallel properties, reconfigurability, simplicity in design, and low cost, FPGAs have been shown to be suitable for the hardware implementation of many signal and image processing algorithms.

Soft morphological filters (SMFs) [10] are nonlinear filters basically based upon order statistics operations. Thus they are computationally expensive [11] especially for SMFs with large structuring functions. This is because calculation of the order statistic operations requires some sorting operation. On the other hand, sorting large number of samples is an exhaustive task because the complexity of any sorting algorithm always depends on the number of samples to be sorted. However, there exist many efficient quick parallel sorting algorithms [12], which are fast and suitable for sorting numbers on parallel architectures. Similarly, the implementation of such algorithms is a function of the input data size and this makes them unsuitable for the calculation of SMFs with large filter dimensions. This is clear in the case of restoration of high resolution images such as HDTV.

Pu [13] proposed a hardware architecture for the implementation of binary soft morphological operations using logic gates. The soft morphological operations were implemented by calculating the weighted order statistic operations of 5-bit binary input image data using a sorting network, which sorted the 5-bit binary data. The sorting network used a compare and swap algorithm.

In [14], Gasteratos proposed an architecture for the realization of soft morphological filters. The technique is based on the majority gate algorithm. Although the processing time of the proposed method is independent of the input data size, additional dummy numbers must be included in the algorithm for the calculation of any order statistic of the input data. However, this is not suitable for the realization of SMFs with large structuring functions in terms of consumption of device resources.

Another approach for the calculation of order statistic operations is a histogram-based method. The method involves summing up the values in the histogram of the input data samples until the desired order statistic is reached. In [15], Gasteratos introduced a fast algorithm for the implementation of weighted order statistic operations based on the histogram-based method. However, instead of adding the local histogram values serially, a successive approximation technique was developed to obtain the order statistic from the histogram in a fixed number of steps. An implementation of this technique on an ASIC [16] is performed for a filter window size of 3×3 . The filter architecture is scalable in terms of pixel resolution and image window size and performs 3.6×10^6 nonlinear operations per second. However, the

performance of any VLSI design is not always guaranteed as the filter size gets larger.

Chakrabarti [17] introduced VLSI architectures for weighted order statistic filters based on a stack filter architecture, array architecture, and sorting network architecture. Also, a comparative study has been performed between the three filter architectures. Implementation results of the three architectures showed that the stack filter architecture required the largest amount of device resources. It was also shown to be faster than the array architecture. For large filter size and pixel resolution, the sorting network architecture was shown to be the smallest in terms of device resources.

In [18], Vardavoulia introduced an architecture for soft colour image morphological operations. The calculation of the soft morphological operations is based on a sorting network. The algorithm uses the merge sort for sorting the values of a structuring element of size 3×2 . The typical operating clock frequency of the circuit is 40 MHz.

Louverdis [19] proposed a hardware implementation of a fuzzy processor suitable for morphological color image processing applications. The proposed hardware structure was based on five functional pipelined stages. The filter architecture is capable of performing standard and soft morphological erosion/dilation for color images of 24-bits using a 3×3 structuring element. The proposed filter architecture was synthesized and implemented on an FPGA. The typical system clock frequency is 65 MHz. The system has shown to be suitable for real time applications.

In this paper, a new FPGA architecture of grey-scale soft morphological filters is proposed. The filter architecture is dependent on a stack filter expression of soft morphological operations with some modification. The architecture ensures that the calculation of the soft morphological operations is independent of the shape and size of the structuring function of the SMF. Examples of filters having structuring functions with different sizes and shapes are demonstrated in Fig. 1. The filter design core is optimized for both time and complexity. The filter is synthesized and implemented on one of SPARTAN FPGA family provided by Xilinx [20].

II. THEORETICAL BACKGROUND

Here we provide an overview to the background and basic definitions of the theoretical aspects that are used in the design of the proposed filter architecture.

1) Grey-Scale Soft Morphological Filters

Soft morphological filters [10] are a class of nonlinear filters. Their definition was originally related to the class of (standard/structural) morphological filters stemming from mathematical morphology. The idea behind soft morphological filters is to relax the standard definitions of morphological filters in such a way as to achieve robustness whilst retaining most of the desirable properties of standard morphological filters. Whereas standard morphological filters are based on local maximum and minimum operations, in soft morphological filters these operations are replaced by more general weighted order statistics.

The key idea of soft morphological operations is that the structuring element is divided into two parts: the hard center which behaves like the standard structuring

element and the soft boundary, where maximum and minimum are replaced by other order statistics. This makes the filters behave less rigidly in noisy conditions and makes them more tolerant to small variations in the shapes of the objects in the filtered image. Before proceeding to the definitions of the soft morphological operations, some concepts have to be considered.

The structuring system $[b, a, r]$ consists of three parameters: functions a and b , having support A and B respectively ($A \subseteq B$) and a natural number, r , satisfying $1 \leq r \leq |B|$, where $|B|$ is the cardinality of B . Function b is called the structuring function, a is its (hard) centre (A is the support of its hard centre), $b|_A$ its soft boundary ($B \setminus A$, the support of its soft boundary) and r is the order index of its center which is also referred to as the repetition parameter.

Let B be a structuring set, with A its center. The fundamental grey-scale soft morphological operations, so-called soft dilation and soft erosion, can be defined as: Grey-scale soft dilation of a signal f by the structuring system $[B, A, r]$ is denoted by $f \oplus [B, A, r]$ and defined as:

$f \oplus [B, A, r](x)$ = the r^{th} largest value of the multiset

$$\{r \circ \{f(x-\alpha) + a(\alpha)\}\} \cup \{f(x-\beta) + b(\beta)\} \quad (1)$$

where $\alpha \in A, \beta \in B \setminus A$

and the symbol \circ is used to denote duplication, for instance

$$n \circ x = \overbrace{x, \dots, x}^{n \text{ times}} \quad (2)$$

Grey-scale soft erosion of a signal f by the structuring system $[B, A, r]$ is denoted by $f \ominus [B, A, r]$ and defined as:

$f \ominus [B, A, r](x)$ = the r^{th} smallest value of the multiset

$$\{r \circ \{f(x-\alpha) - a(\alpha)\}\} \cup \{f(x-\beta) - b(\beta)\} \quad (3)$$

where $\alpha \in A, \beta \in B \setminus A$

The filter parameters are the size and shape of the filter soft boundary, the shape of the hard center, and the filter rank. The soft morphological operations are selected from the set $\{\text{soft-erode}, \text{soft-dilate}\}$.

2) Stack Filters

Stack filters are a class of nonlinear filters, first introduced by Wendt et al [21]. All stack filters have two properties, a superposition property known as threshold decomposition and an ordering property known as the stacking property.

The threshold decomposition is first achieved for each pixel of the input window as follows:

Consider a vector of grey-scale values $x = (X_1, X_2, X_3, \dots, X_N)$, in the range $X_i \in \{0, 1, \dots, M-1\}$. The threshold decomposition of x amounts to expressing it as $M-1$ binary vectors x^1, x^2, \dots, x^{M-1} defined by

$$x_n^m = \begin{cases} 1 & \text{if } X_n \geq m \\ 0 & \text{otherwise.} \end{cases} \quad (4)$$

A positive Boolean function $g(\cdot)$ is then applied at every threshold level. The stack filter $S(\cdot)$ is characterized by its positive Boolean function $g(\cdot)$ applied at every threshold level m as follows:

$$S(x) = \sum_{m=1}^{M-1} g(x^m) \quad (5)$$

As mentioned above, the binary function that is applied at each threshold level should obey the stacking property. All positive Boolean functions (PBFs) satisfy this constraint. A PBF is a Boolean expression (function) that does not contain any complemented variables. For example, the function $x_1 + x_2 x_3$ is not a PBF whilst the function $x_1 + x_2 x_3 + x_1 x_3$ is a PBF and it corresponds to $\max(x_1, \min(x_2, x_3), \min(x_1, x_3))$. Usually, the same PBF is applied to the binary sequence, which results from threshold decomposition of the inputs, at each threshold level.

3) Stack Filter Expressions of Soft Morphological Filters:

It has been shown in [22] that soft morphological operations can be represented by stack filters and performed using threshold decomposition so that the soft morphological operations will be calculated in the binary domain instead of the grey-scale domain. So, the relation between stack filters and soft morphological operations is introduced in [22] as follows:

Let B be a structuring set with A its center. Then the positive Boolean function that corresponds to stack expression of

a) Soft dilation, $f \oplus [B, A, r]$ is

$$g_d(x) = \sum_{\alpha \in A} x_\alpha + \sum_{\substack{I \subset B \setminus A \\ |I|=r}} \prod_{\beta \in I} x_\beta \quad (6)$$

b) Soft erosion, $f \ominus [B, A, r]$ is

$$g_e(x) = \sum_{\alpha \in A} x_\alpha \cdot \sum_{\substack{I \subseteq B \setminus A \\ |I|=|B \setminus A|+1-r}} \prod_{\beta \in I} x_\beta \quad (7)$$

III. FILTER ARCHITECTURE

The proposed architecture of the SMF design core is based on a stack filter expression and the binary tree search algorithm [23]. It should be noted that, it is only possible using a stacking filter to compute a SMF with a 'flat' structuring element [22]. However in this case we employ it with a non-flat structuring element and the stack filter is used solely to determine the r^{th} rank of the soft boundary of the SMF. The block diagram of the proposed filter architecture is shown in Fig. 2. The SMF architecture consists of three main functional modules: Grey-level shift and truncation module, order statistic module, and output module. All filter design stages are synchronized with the global clock.

Image data and filter data are stored in registers. The design has 27 registers for storing image data each of 8-bit width and another 27 registers for accommodating the structuring function of the SMF each of 3-bit width. The order index and the soft morphological operation are also stored in registers. All registers are connected to the inputs of the first module.

1) Grey-level Shift and Truncation Module

This module performs the grey-scale addition/subtraction operations for soft-dilation/soft-erosion respectively. Then the result is truncated to be within the grey-scale range of the input image, 0 to 255. Also, if the value in the soft boundary of the SMF is equal to the out of support value then the output is set to "0". The output is stored in 27 registers each of 8-bit width. The data stored in the register are fed to the input of the second module.

2) Order Statistic Module

The main function of this module is to calculate the order statistic value of the soft boundary of the SMF. This is performed by two cascaded operations. The first operation involves thresholding the input samples to the module. This is carried out by comparing all the input values with the current threshold such that the result is "1" if the input value is greater than or equal to the current threshold value and "0" otherwise. The results are stored in a pipeline register. Pipelining is a technique whereby operations are divided into small primitive operations, store the results of each operation in a register, and continue the calculation in the next clock cycle. This enhances the overall processing time of the design.

The second operation is concerned with the calculation of the PBF at the current threshold. This is achieved by summing up all the registered outputs of the threshold decomposition operation, using the majority gate [24], and comparing the result with the order index of the SMF such that if it is greater than or equal to the order index the result is "1" otherwise the result will be "0".

3) Output Module

Stacking PBFs at all threshold levels is the final step of the implementation of a stack filter. This requires the calculation of a number of PBFs equals to $2^b - 1$, where b is the pixel resolution. For high resolution images this number will be very large. For example, for 8-bit images the required number of PBFs is 255 and hence a matrix of $|B/A| \times 255$ bits. This consumes a huge amount of device resources.

The threshold decomposition of SMFs requires the implementation of the same PBF at each threshold level, which leads to the construction of the so-called homogenous stack filter [22]. This property guarantees that if at any threshold the PBF value is '1' then all the preceding thresholds must have PBFs each with value '1'.

To make use of the homogeneity of the stack filter, the binary tree search [23] is used to compute the output value of the stack filter. The algorithm requires the implementation of only one PBF and the stack filter output is completed in b serial operations.

Then the output module performs a comparison between the order statistic value and the center pixel output from the first module (center pixel after grey-level shift and truncation) such that it computes the maximum/minimum of the two values for soft-dilation/soft-erosion. Also, if the center pixel is out of support of the structuring function's overall support the output value is taken as the order statistic value.

Because the maximum allowable clock frequency is an important factor for a good FPGA design, the SMF design core is pipelined to achieve high internal clock frequency. Hence, it is clear that the filter is efficient in terms of both hardware complexity and processing time.

IV. SYNTHESIS AND IMPLEMENTATION RESULTS

The proposed filter design calculates the soft morphological operations of a grey-scale SMF of spatial dimensions of up to 5×5 or of spatio-temporal dimensions of up to $3 \times 3 \times 3$ with image resolution of 8bpp. The SMF core is programmed through the hardware description language, VHDL [25]. The filter design has been synthesized by means of logic gates and arithmetic functions such as comparators, data registers, adders, subtractors, and multiplexers. Fig. 3 shows the layout of the SMF implemented on the SPARTAN-II XC2S150 FPGA architecture. The SMF design core is optimised for both complexity based on the number of FPGA slices required, and processing time, calculated as the total number of clock cycles required to filter one pixel. The SMF design uses 46% of the total number of slices and runs with clock speed up to 40 MHz. This has been achieved by pipelining. This reflects how much the proposed design reduces the device area used by the filter, while keeping high internal clock frequency. The entire filtering process takes only 18 clock cycles per pixel. So, an image of 256×256 pixels could therefore be easily filtered at 30 frame/s. This processing time is dependent only on the pixel resolution and independent of the size and shape of the structuring function of the SMF.

V. CONCLUSION

In this paper, FPGA architecture of grey-scale soft morphological filters is proposed. The architecture is based on a stack filter expression of soft morphological filters with some modification. The proposed filter architecture guarantees fixed processing time

independent of the size and shape of the structuring function of the filter. The filter architecture is pipelined to achieve high internal clock frequency. The filter design calculates grey-scale soft morphological operations of maximum filter dimensions of $3 \times 3 \times 3$ with pixel resolution of 8 bits. The filter also includes all smaller filters with any size and shape inside this domain and operates with a typical clock frequency of 40 MHz. Synthesis and implementation results showed that the proposed filter architecture is suitable for the restoration of digitised image sequences in real time.

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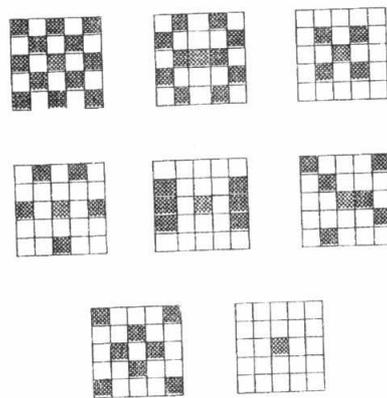


Fig. 1 Examples of filters having structuring functions with different shapes and sizes.

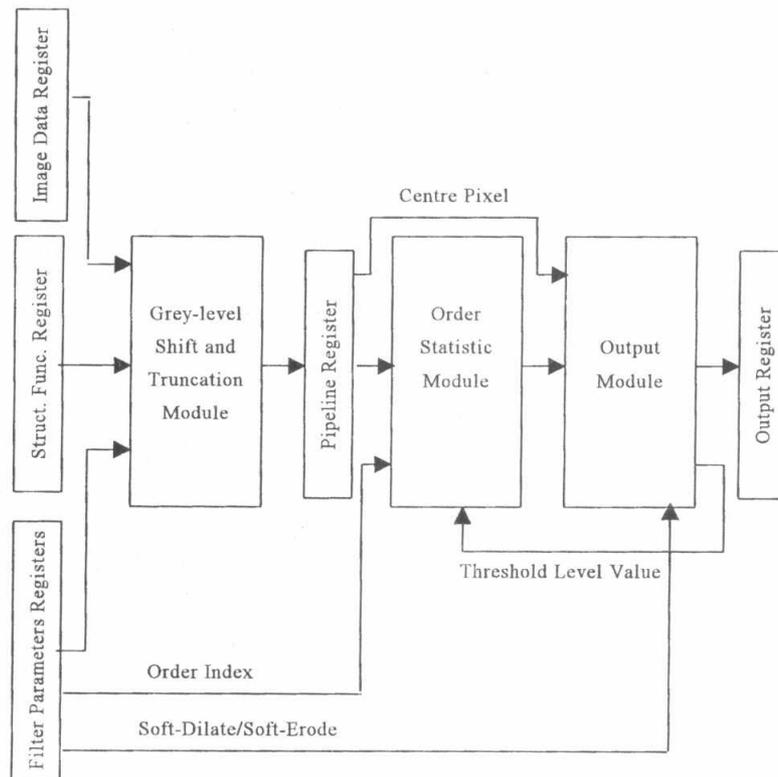


Fig. 2 Soft morphological filter architecture.

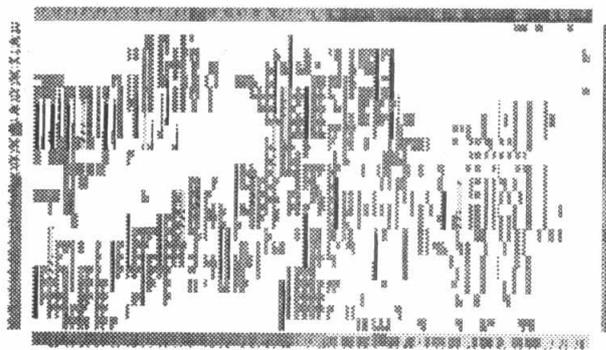


Fig. 3 Layout of the proposed filter design.