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A BALANCED ACTIVE POWER DIVIDER FOR COHERENT DISTRIBUTION OF LOCAL OSCILLATOR SIGNAL IN A PLANAR TRANSMITTING-RECEIVING ARRAY

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ABSTRACT

This paper describes the design of a balanced signal distribution system to feed an n by n set of mixers with local oscillator signals equal in frequency, phase and magnitude. This system is used in a planar n by n receiving/ transmitting array that measures and/or controls the direction of arrival of the received/transmitted signals. The design steps are clearly described. Optimization goals and variables are specified and the results of linear, electromagnetic and combined simulations are given and compared. The final product layout is shown and its performance is described. This paper is a typical example of a successful computer-aided design which saves time, effort and money before manufacturing a prototype. It introduces the active power divider as a zero-loss signal distribution device.

KEY WORDS

Power divider, phase unbalance, amplitude unbalance, electromagnetic simulation, combined linear-electromagnetic simulation, CAD, Microstrip, characteristic impedance, matching transformer.

NOMENCLATURE

$\{S_{ij}\}$ = *set of scattering parameters*
L_iS = *sub circuit at the* i^{th} *level*
Z_i *and* Z_o *input and output impedances*

INTRODUCTION

To determine the direction of arrival of a signal, a linear array receives the signal with its different elements and compares their relative phases. Due to cost and availability problems of phase detectors at higher microwave frequencies, the received signals are usually down-converted into a lower frequency band where their phases are

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compared. The basic idea is that the phase difference between two signals does not change if both are frequency-translated with the same shift. Any phase unbalance in the frequency translation process severely affects the reliability of the whole process. Amplitude balance is also required to guarantee equal driving powers for mixers and, consequently, equal input signals to different phase detectors. The size of the problem increases when we speak about a planar receiving array. When the same principle is used to build a repeater system with receiving and transmitting planar arrays, it is evident that we need a system of precise active power dividers with controlled phase and amplitude balance and power gain to distribute the local oscillator signal on all mixers of the receiving and transmitting arrays with equal phases and amplitudes. Those active power dividers are the subject of this paper.

DESIGN OF 8-WAY PASSIVE POWER DIVIDER

The three-port power divider originated from Wilkinson [1] who described a circularly symmetric power divider, which split a signal into equi-phase–equi-amplitude signals with an even or odd number of n. With n = 2, Wilkinson's power divider could be a three-port power divider achieving a perfect isolation at one frequency [3]. Fooks and Zakarevicius analyzed a classical Wilkinson power divider as a four-port network, one of which terminated with a resistor [2]. Recent research works concentrate on increasing the frequency band of power dividers [4,5], decreasing their size [6,7] or generating unequal output powers. Since our application needs none of these requirements, we are going to proceed with a classical Wilkinson power divider design.

It is required to design and implement an eight-way active power divider with zero loss, zero phase unbalance and minimum amplitude unbalance at a certain local oscillator frequency. This power divider will be repeated eight times to feed a planar 8 by 8 receiving array in the x frequency band. Let the local oscillator frequency be 7.5 [GHz]. We designed an eight-way passive power divider. We optimized the design for input and output matching, isolation between adjacent outputs, minimum phase and amplitude unbalances and mechanical requirements of the planar array system. We measured the insertion loss of the power divider and compensated it by an amplifier-attenuator set to get a final zero power loss.

First Design Run

We started by designing a two-way Wilkinson power divider on an RTDuroid6002 substrate with a 2.94 relative dielectric constant and 0.508 [mm] height. For this substrate, a 50-Ohm line width is 1.29 [mm]. A classical Wilkinson power divider consists of two $\lambda/4$ impedance transformers and a $2Z_0$ termination resistor. An input-output line width of 1.344 [mm] and a 0.679 [mm] branch line width gave a good linear simulation result. Then, a planar electromagnetic simulation and a combined linear-electromagnetic simulation were done with the Eagleware GENESYS2004 CAD software package. The schematic and layout diagrams of the two-way power divider are shown in Fig.1, while Fig. 2 shows the electromagnetic simulation results which gave satisfactory results (S11 better than -16 dB, S22 about -29 dB, S21 better than -3.3 dB and isolation between output ports better than 24 dB at the desired frequency).

We constructed a four-way power divider by cascading two power dividers to the output ports of the first. Then, we extended the idea by cascading a 2-way power divider to each output of this 4-way divider. The functional diagram is shown in Fig.3 below, where seven different 3-port sub-circuits can be recognized. The first is the 2-way divider shown in Fig.1 with two variables to be optimized; namely lengths Lo, L1. It was denoted Level-1 sub-circuit (L1S). The second level sub-circuits (L2S), repeated twice in the diagram, had the variable length L2. The third level sub-circuits (L3S), repeated four times, had the variable length L3. The transmission lines at the output ports of each sub-circuit had the same variable width w_5 while the line widths of all impedance transformers had the same variable width w_7. We adjusted the lengths of the two output arms at each level to guarantee certain separations among the output ports determined by the system mechanical requirements.

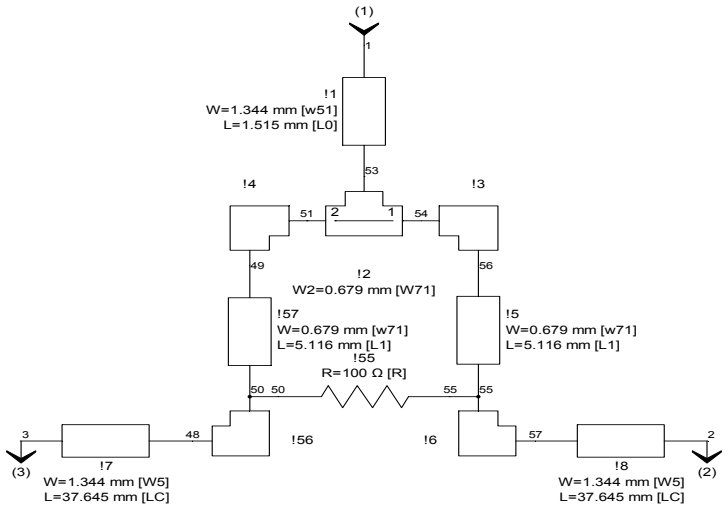

Fig.1. A two-way Power Divider

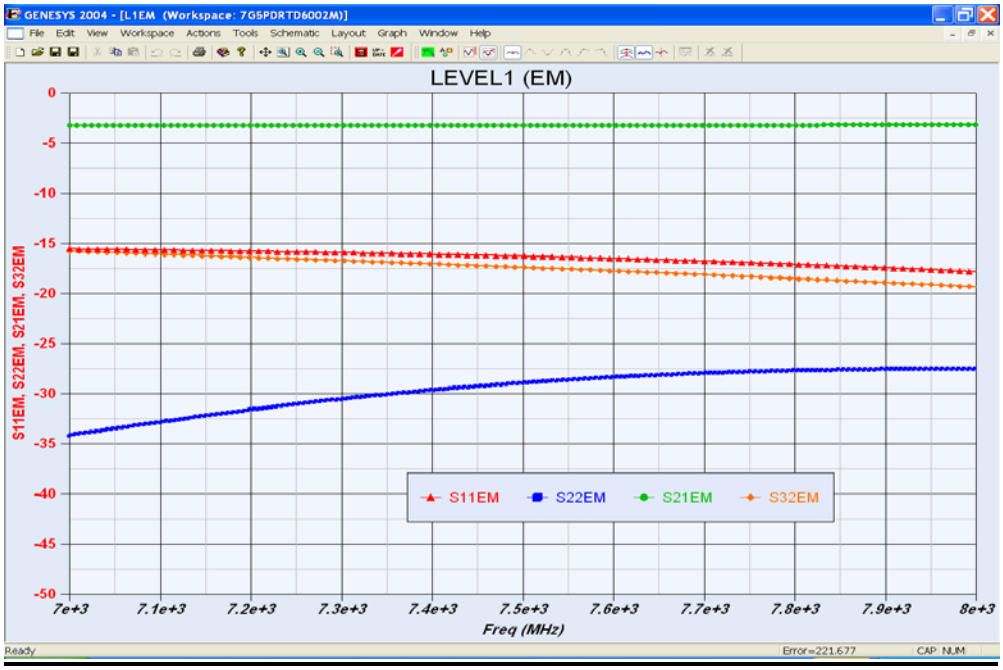

Fig.2. Electromagnetic Simulation Results of the two-way Power Divider

We run a multi-objective optimization process with 6 variables on the whole circuit with the following simultaneous goals:

S_{11} < -25 dBm 7.40 [GHz] < f < 7.60 [GHz]
S_{22} < -30 dBm 7.40 [GHz] < f < 7.60 [GHz]
S_{32} < -25 dBm 7.40 [GHz] < f < 7.60 [GHz]
Z_o (L1s) = Z_i (L2s) = 50 [Ohms] 7.48 [GHz] < f < 7.52 [GHz]
Z_o (L2s) = Z_i (L3s) = 50 [Ohms] 7.48 [GHz] < f < 7.52 [GHz]

where

Z_o (L1s) = output impedance of the first-level divider
Z_i (L2s) = input impedance of the second-level divider
Z_o (L21s) = output impedance of the second -level divider
Z_i (L3s) = input impedance of the third-level divider

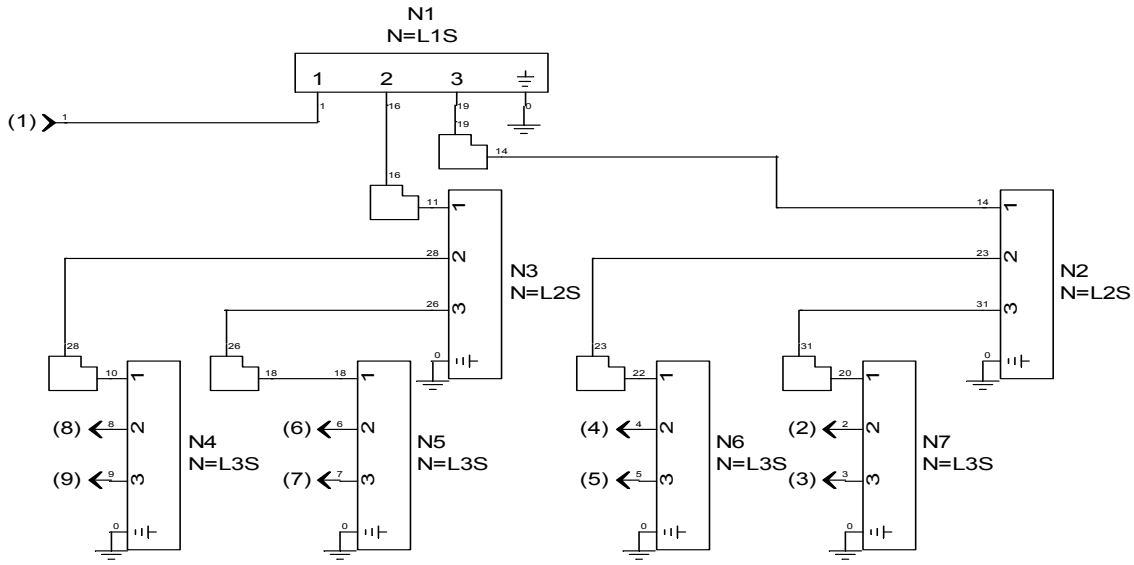

Fig.3. Cascading 2-way power dividers to construct an 8-way power divider

The results of matching optimization among the three divider levels is shown in Fig.4 below. It can be noticed that the matching is not yet perfect. The performance of the whole power divider circuit is shown in Figure 5 as a result of the linear simulation. The layout of the eight-way power divider was constructed and a combined EM simulation was performed for each level separately and then for the whole power divider. The layouts and EM simulation results are shown in Fig. 6. A photograph of the implemented power divider is shown in Fig. 7. One of the reasons of deviation between the EM and linear simulation results is the mutual coupling between the two matching transformer lines at each level which does not appear in linear simulation.

It is worth noting that the EM simulator approximates conductor boundaries to the resolution mesh set by the user. We set the resolution mesh to 0.2 [mm] horizontally and 0.28 [mm] vertically; in order to use a reasonable memory size of less than 700 Mega Bytes. We run the EM simulation on 11 different frequencies from 7 GHz to 8 [GHz]. The run took more than 35 [sec] per frequency on a Sempron processor.

Second Optimization Run

To enhance the performance, we increased the distance between the two matching

transformer lines of the first stage. We increased the number of design variables and optimized each stage separately. We introduced w71, w72 and w73 as variable transformer line widths for the three stages, respectively. We run three independent optimization processes on the three divider-levels. The results are shown in Fig. 8.

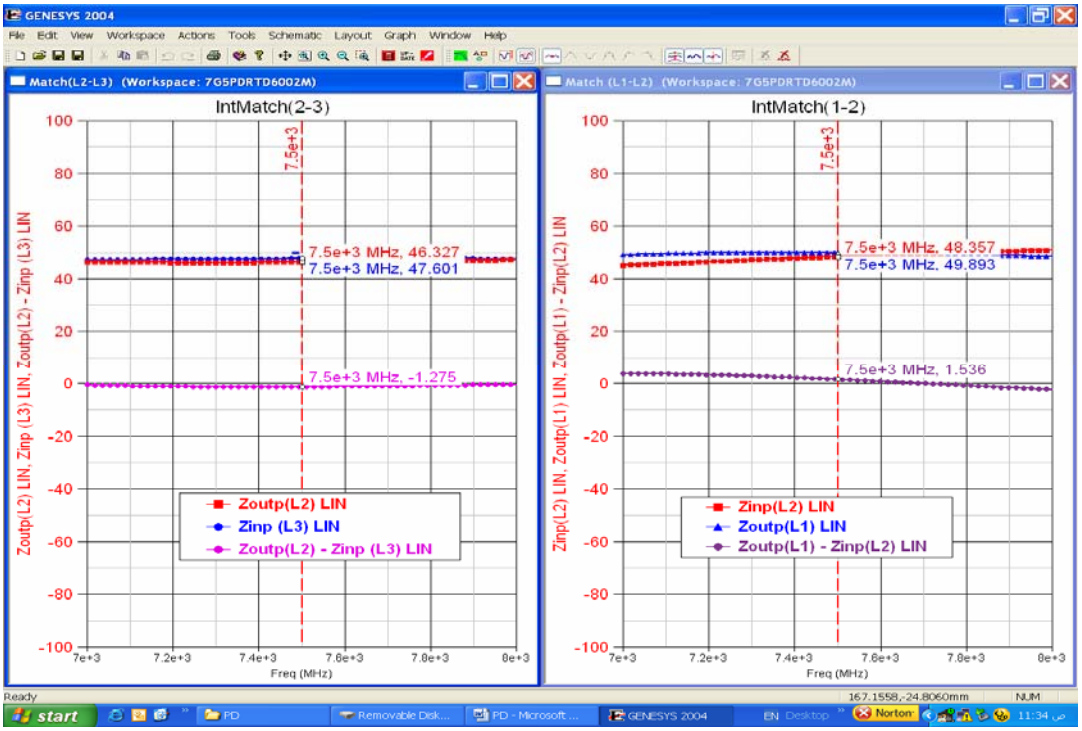

Fig.4. Inter-stage Matching

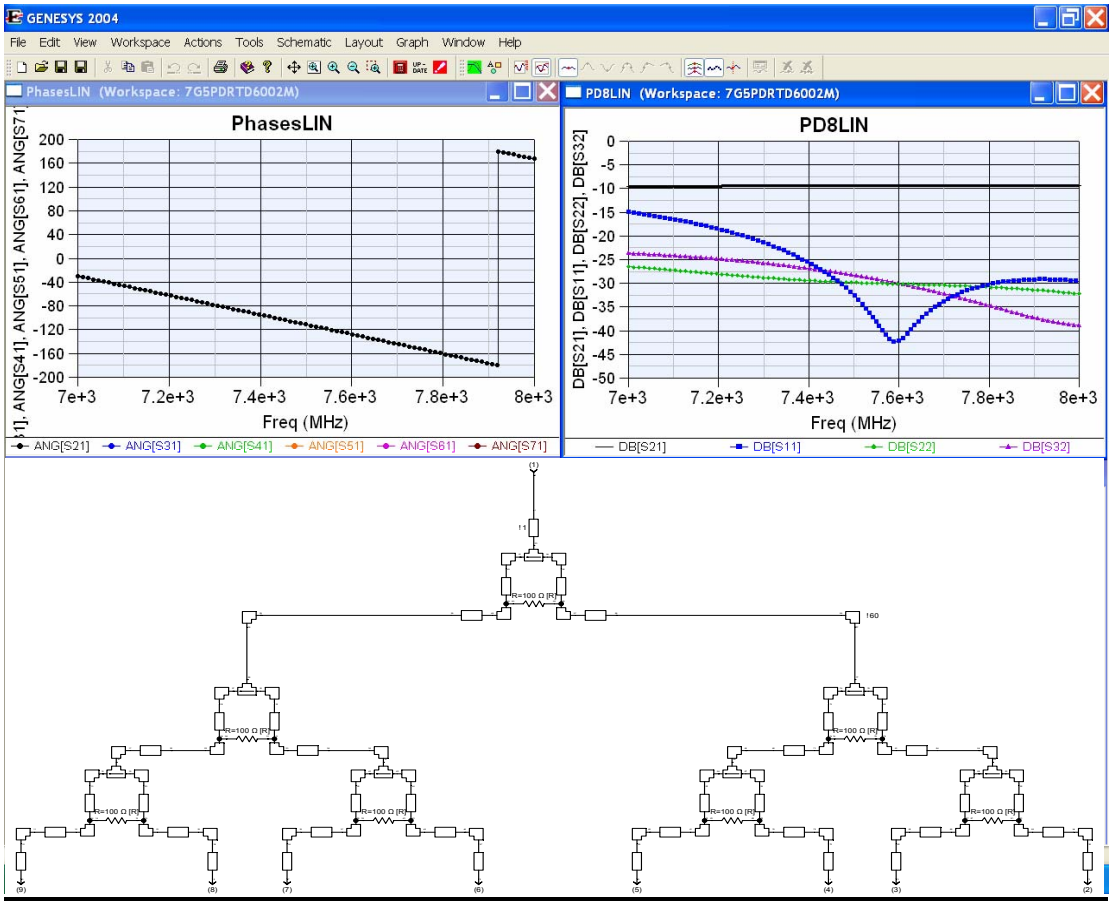

Fig.5. First Run Optimized Linear Simulation

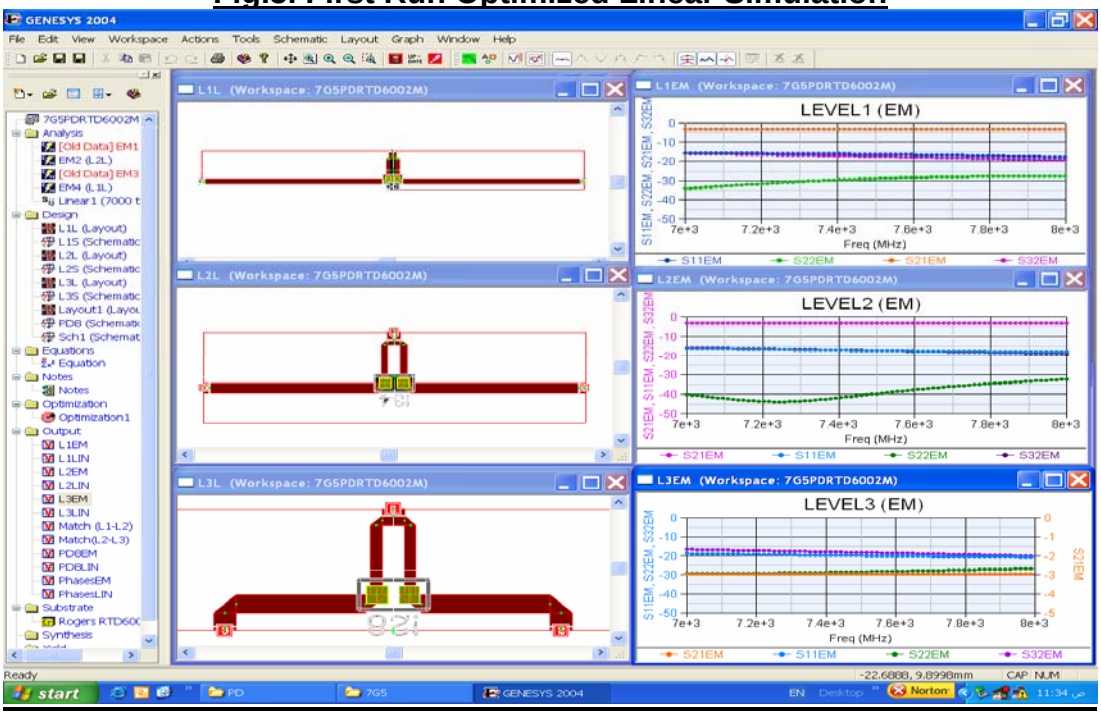

Fig.6. Layout and EM simulation
a. at different levels b. the whole power divider

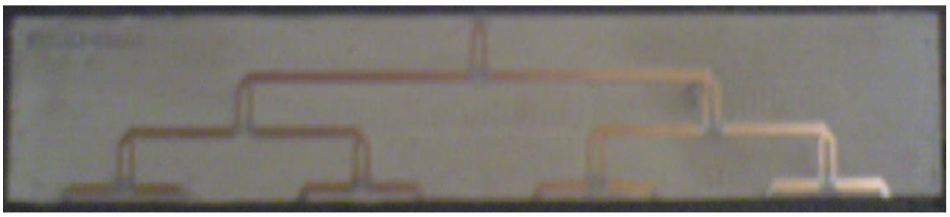

Fig.7. PCB Implementation of the 8-way power divider

A big enhancement can be observed in the performance of each divider level. Moreover, we can clearly recognize that the overall performance of the divider became much better due to the independent optimizations on the three levels. A perfect matching between each two subsequent stages was achieved and both s_{11} and s_{22} became better than -30 [dB]. Even the isolation between two subsequent outputs became better than 30 [dB].

The last step was the combined EM-LIN simulation to verify the design. Fig. 9 shows the results of combined simulation for the complete power divider. We can recognize better input and output matching (s11 and s22 about 20 dB) and better output port isolation (better than 25 dB) compared to the EM simulation of the first run. The total insertion loss of the power divider is less than 0.4 dB above the 9 dB of an ideal 1:8 divider and the maximum amplitude unbalance < 0.212 dB and maximum phase unbalance < 4 °. We can safely say that this unbalance is due to the EM simulator approximation and that the electrical lengths of the eight paths are exactly equal.

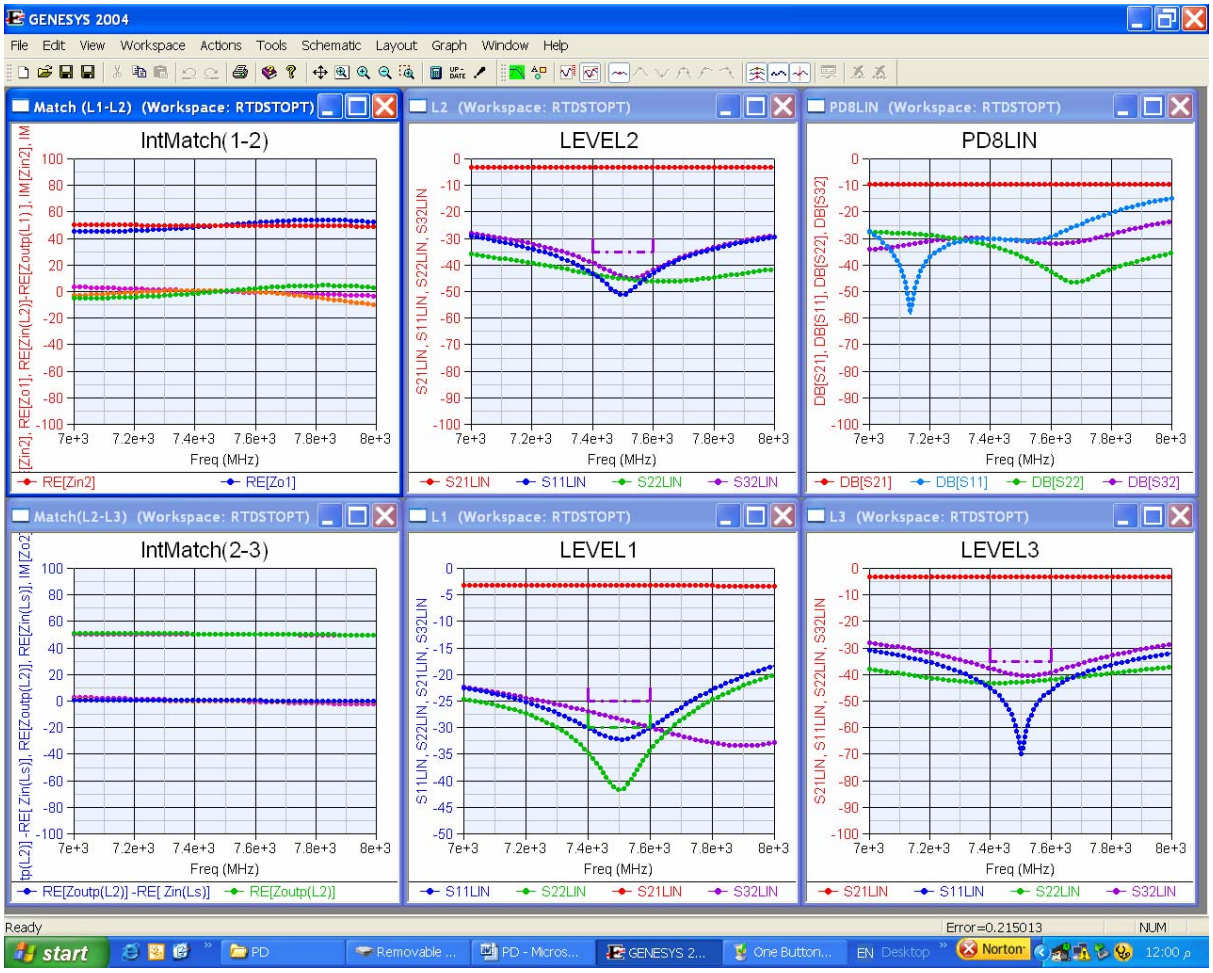

Fig.8. Results of the second optimization run

AMPLIFIER-ATTENUATOR DESIGN

The last stage is to design an amplifier-attenuator setup to compensate for the total power divider loss and get a zero overall insertion loss. We selected an internally-matched amplifier IC (the GALI-1 of MiniCircuits products). The specified gain at 7.5 GHz is about 11 dB, while the power divider loss was about 9.2 dB. We neede an attenuator after the amplifier. We designed a 1.8 dB resistive PI attenuator on the microstrip transmission line with 50 Ohm input and output impedances. Combined linear-electromagnetioc simulations showd that a simple series resistor can do the job without affecting the output matching of the amplifier as shown in Fig.10a. We adopted the second solution because of its smaller size. The amplifier design is shown in Fig. 10b.

Amplifier Bias Calculation:

$$V_c = V_{cc} - I_c.R_c = 9 - 0.04 * R_c \qquad (1)$$

We select a 9 [v] power supply to secure a wide temperature range operation. If we take R_c = 132 [Ohms]; the V_c becomes 9 - 0.04 * 132 = 9 - 5.28 = 3.72 [v] which is in the recommended range for GALI-1 [3.0 < Vc < 4.1]. The power dissipation will be

0.2112 [w]. We recommend a parallel combination of a 220 [Ohm]-0.25 [w] 1206 case and a 330 [Ohm]-0.25 [w] 1206 case resistor.

Fig.9. Layout and Combined simulation results after optimization

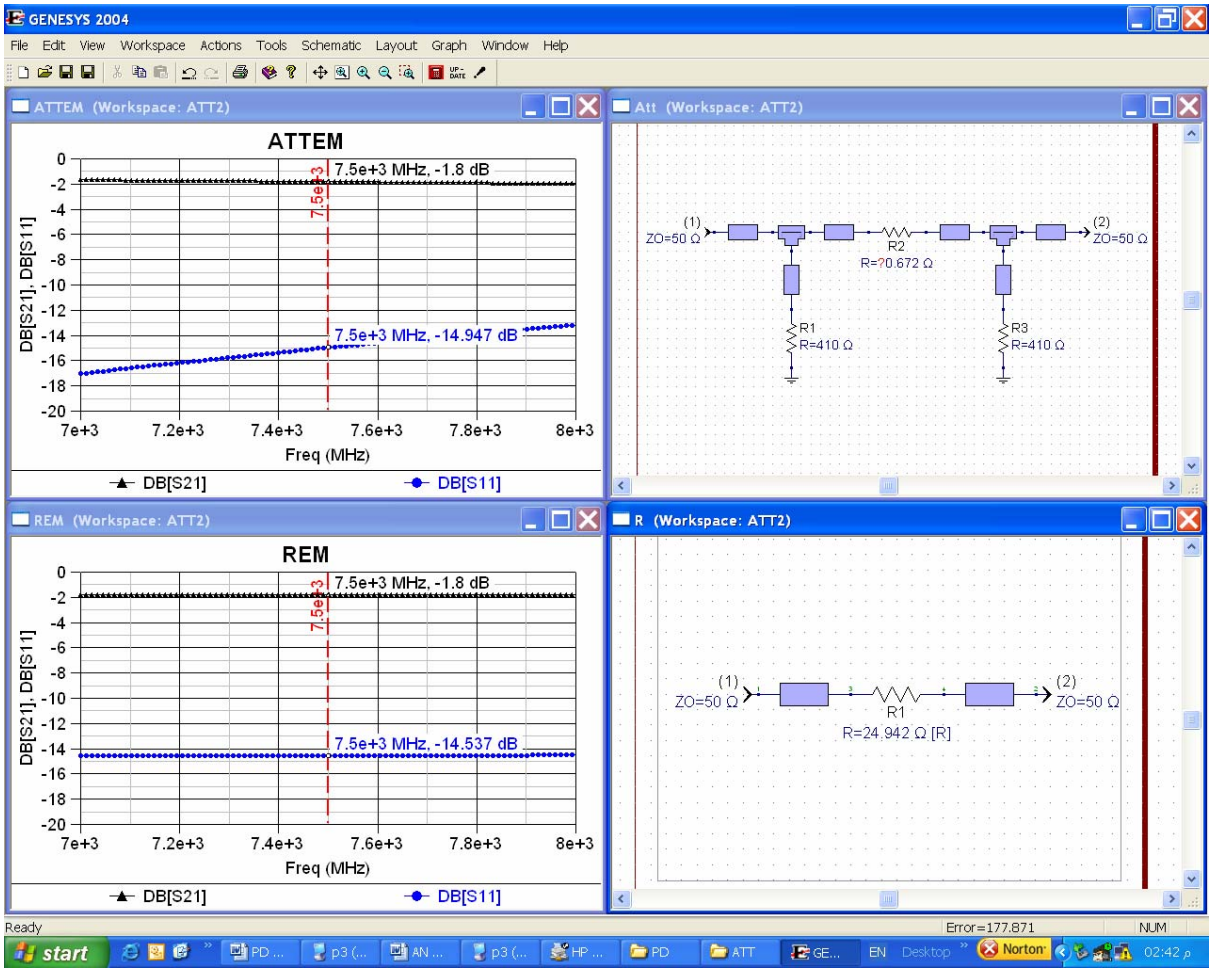

Fig.10a. A comparison between a PI and a single resistor attenuators

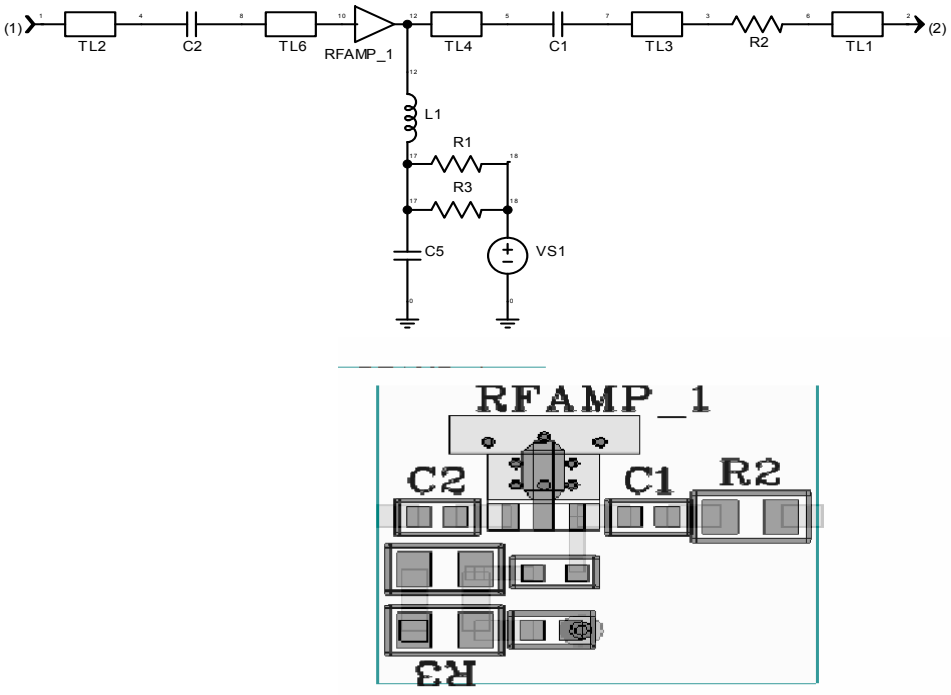

Fig.10b. Ampliffier Design

LO DISTRIBUTION SYSTEM FOR AN 8X8 ARRAY

Fig. 11 shows a functional diagram of such a system, composed of 9 identical modules. Each module is the active power divider with zero loss, minimum amplitude and phase balance that has just been designed and implemented.

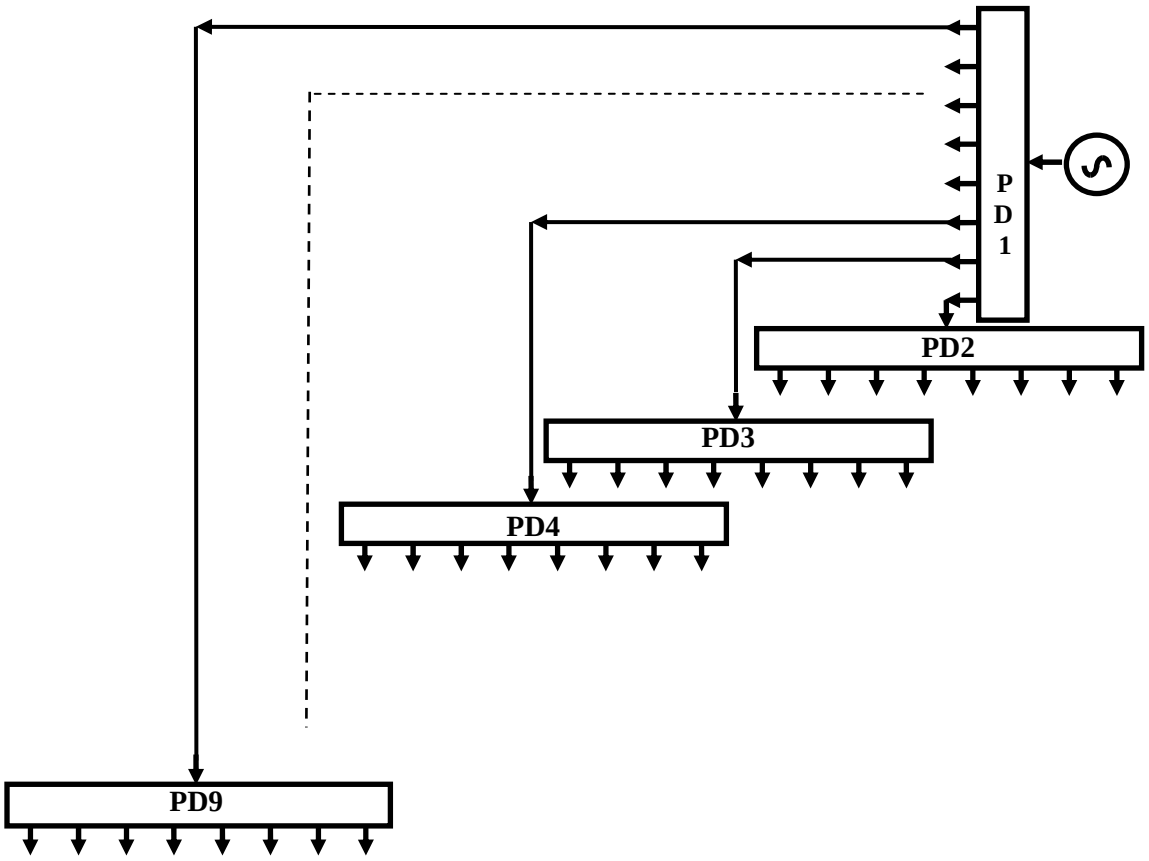

Fig.11. Local Oscillator Distribution System for an 8x8 array

CONCLUSION

1. An 8-way active power divider has been designed and implemented with zero loss and balanced phases and amplitudes. This active power divider can be used to distribute a single local oscillator signal on a set of different identical mixers to perform a coherent frequency translation in a linear transmitting/receiving array.
2. It can be repeated 9 times to perform the same function in an 8x8 planar array.

ACKNOWLEDGMENT

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