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Design and Simulation of DVB-T2 Transmitter

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Abstract: Digital video broadcasting, DVB has become the synonym of digital television as well as data broadcasting. The DVB Project was launched on the 10th of September, 1993. DVB systems distribute data using a variety of approaches. These approaches include: satellite, cable and terrestrial television. These three sub-standards are basically differ in the specifications of the physical representation, modulation, transmission as well as reception of the signal. DVB-T is the consortium standard for broadcast transmission of digital terrestrial television. The key motivation behind this standard was the desire in several European countries to offer high definition television (HDTV) services as efficiently and effectively as possible.DVB-T2 is considered to be the modified version of DVB-T.DVB-T2 leads to performance improvement by introducing state-of-the art communication techniques where it achieves 30% better capacity compared with DVB-T. In some cases, the data rate will be up to 50% higher under comparable conditions. In this paper we demonstrate the architecture of the DVB-T2 system, as well as a MATLAB design and simulation of the DVB-T2 transmitter. The transmitter model is then tested for different data rates. The model provides an overall evaluation of the DVB-T2 transmitter parameters and can be used for educational and testing purposes.

Keywords: Bit interleaver, rotated constellation, cyclic delay, OFDM

1. Introduction

Digital Video Broadcasting (DVB) is an industry led consortium of over 280 broadcasters, manufacturers, network operators, software developers, regulatory bodies and others in over 35 countries committed to designing open interoperable standards for the global delivery of digital media services. They are published by a Joint Technical Committee for Electro technical Standardization Committee European de Normalization Electrotechnique (CEBELEC) and European Broadcasting Union (EBU) Digital video broadcasting (DVB) is a family of standardized technologies designed to facilitate broadcasting of images, sound, multimedia and to permit a large degree of user interaction. The most common standards adopted by DVB organization are DVB-T (Digital Video Broadcasting – Terresital) standard, DVB-C (Digital Video Broadcasting - Cable) standard, DVB-S (Digital Video Broadcasting - Satellite)standard and DVB-H (Digital Video Broadcasting - Handheld) standard .Many of these standards are patented. (Digital Video Broadcasting – Second Generation Terrestrial) is the extension of the television standard DVB-T where they are based on the purpose of supporting High Definition Television (HDTV) services The characteristics of DVB-T2 are a concatenation of Bose-Chaudhuri Hocquenghem (BCH) as outer codes and Low Density

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Parity Check (LDPC), as inner codes with word length up to 64,800 bits, enabling significant proximity to Shannon limit. Higher order modulations range up to 256-QAM while OFDM includes as many as 32,768 subcarriers [1].The DVB-T2 system high level architecture is shown in Fig. 1.

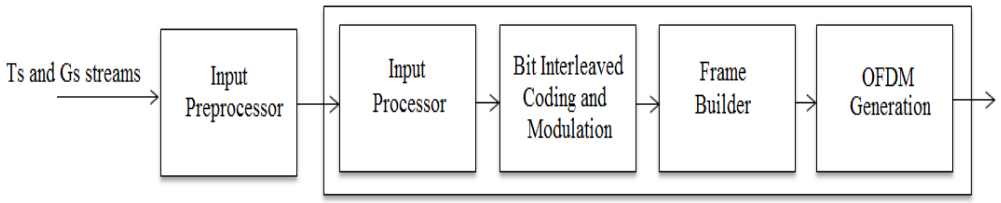

Fig. 1 High Level Architecture of DVB-T2 system

The DVB-T2 system consists of four main blocks which are the input processor, bit interleaved coding and modulation, frame builder and OFDM (Orthogonal Frequency Division Multiplexing) generation blocks .The preprocessor block is not a part of the system. Were it prepares the data (Ts or Gs streams) for the DVB-T2 system. It may include a Service splitter or de-multiplexer for Transport Streams (TS) to separate the services into the T2 system inputs, which are one or more logical data streams. These are then carried in individual Physical Layer Pipes (PLPs) [2].Many aspects of the DVB-T2 system had been discussed in previous papers like the constellation rotation [3], the bit interleaver [4][5][6],the implementation of the channel coding on FPGA[7] and many others. In this paper, we will consider the implementation of the hardest blocks of the DVB-T2 system using the Matlab program taking the condition of a single PLP (Type A). The rest of the paper is organized as follows: In section 2, the proposed system modules are discussed. In section 3, the implementation of the proposed system is given .In section 4, the output results are shown. Finally; the conclusion is given in Section 5.

2. Proposed DVB-T2 Transmitter Modules

In this Section a DVB-T2 transmitter model is considered as in [2]. The detailed block diagram is shown in Fig. 2.

The first block of the system is the input processor block it is split into two main functions (mode adaption, and stream adaption).The mode adaption function consists of three blocks the input interface, CRC-N encoder and the BB-header (Baseband-header), while the stream adaption consists of two blocks, the padding insertion and the BB-scrambler (Baseband-scrambler) .The input to the input processor block is a single stream (PLP) .The mode adaptation module slices the this stream into data fields which after stream adaptation, will form BBFRAMEs (Baseband frames) of K_{BCH} bits .The information frame from the input interface goes through the FEC (Forward Error Correction) encoder of an outer coder (BCH), and an inner Coder (LDPC) to generate the codeword N_{LDPC}.

Afterwards; this sequence is interleaved using the bit interleaver which consists of two cascaded interleavers:

1) A parity interleaver which divides the parity bits of FEC block into 360 blocks (This is constant for all rates) of Q_{LDPC}bits (Every rate has different Q_{LDPC} values) [2] and then interleaves them as seen in Fig. 3.

2) A column twist interleaver which interleaves all the bits by writing them column wise (N_c) and serially reading them out row-wise (N_r) with twisted start positiont_c, as shown in Fig.4 where N_r,N_c, and t_c are specified according to the implemented modulation technique [2].

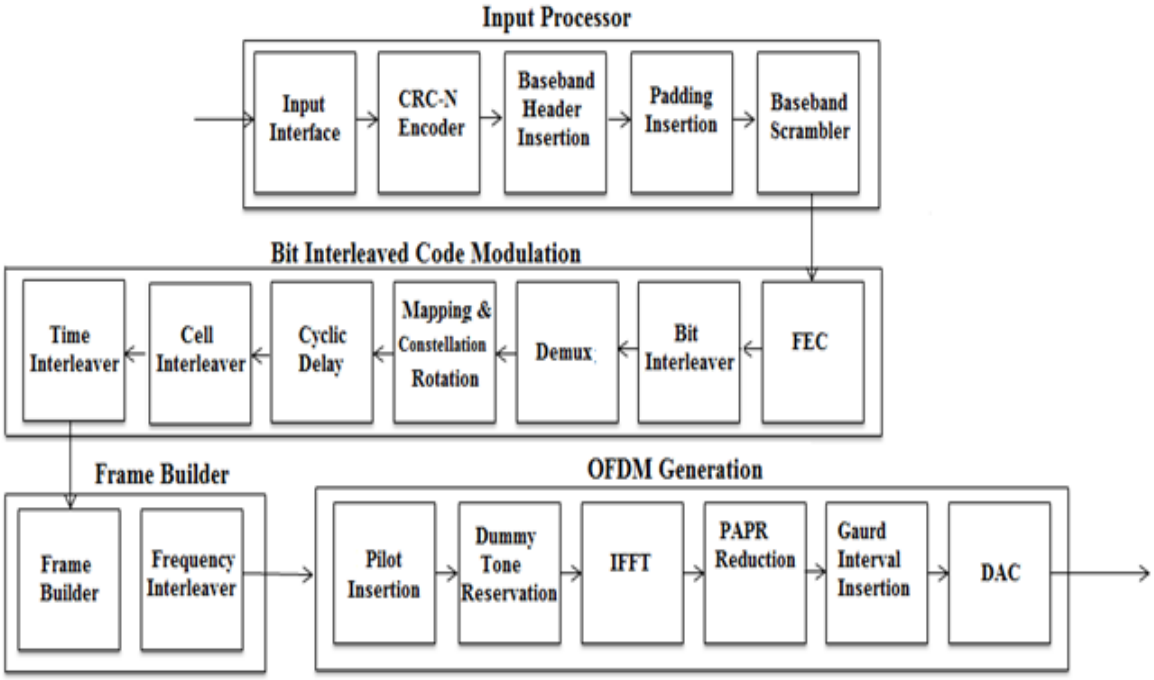

Fig. 2 Block Diagram of DVB-T2 system

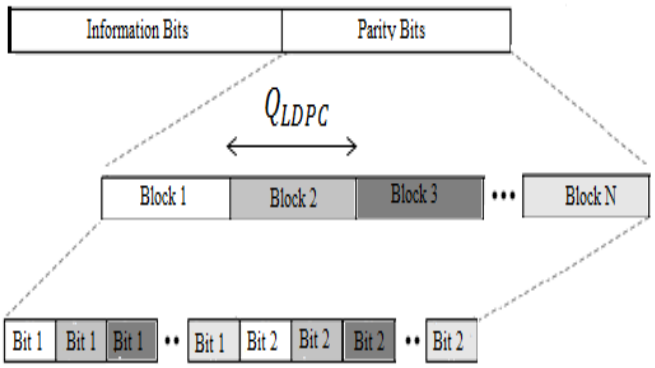

Fig. 3 Parity Interleaver Algorithm

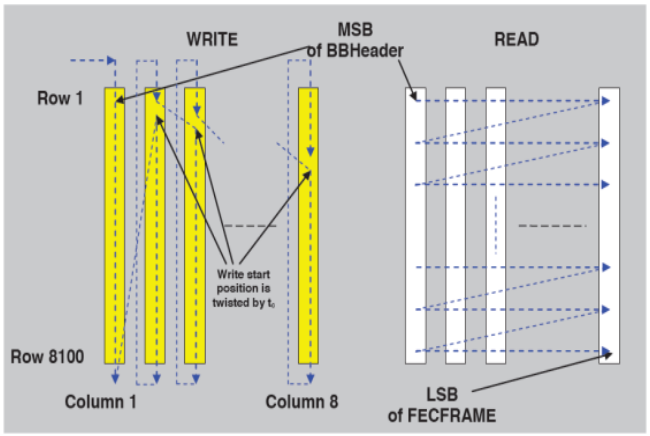

Fig. 4 Column twist algorithm

The output stream of the bit interleaver block is demultiplexed into n substreams. Each substream shall be modulated using either Q-PSK, 16-QAM, 64-QAM, 256-QAM constellations. The DVB-T2 system addresses a rotation to the constellations of the Qam (Quadrature Amplitude Modulation) mapper so that I and Q channels can be mapped separately as two independent PAMs where the correlation between them makes each metric computed over two dimensions corresponding to the I and Q components of the rotated constellation signal. [3]. Then the imaginary part is cyclically delayed by one cell within a FEC block. The cell interleaver shall uniformly spread the cells in the FEC codeword, to ensure in the receiver an uncorrelated distribution of channel distortions and interference along the FEC codewords .These cells shall be grouped into interleaving frames by the time interleaver to be given to the frame builder. The frame builder prepares data for the OFDM generation by mapping cells of the time interleaver to frames where T_F is the frame duration, T_S is the total OFDM symbol duration and T_{P1} is the duration of the P1 symbol, and $T_{SF}$is the super frame duration as seen in Fig. Then the frequency interleaver takes the data from each frame and maps it onto the carriers in each OFDM symbol [2].

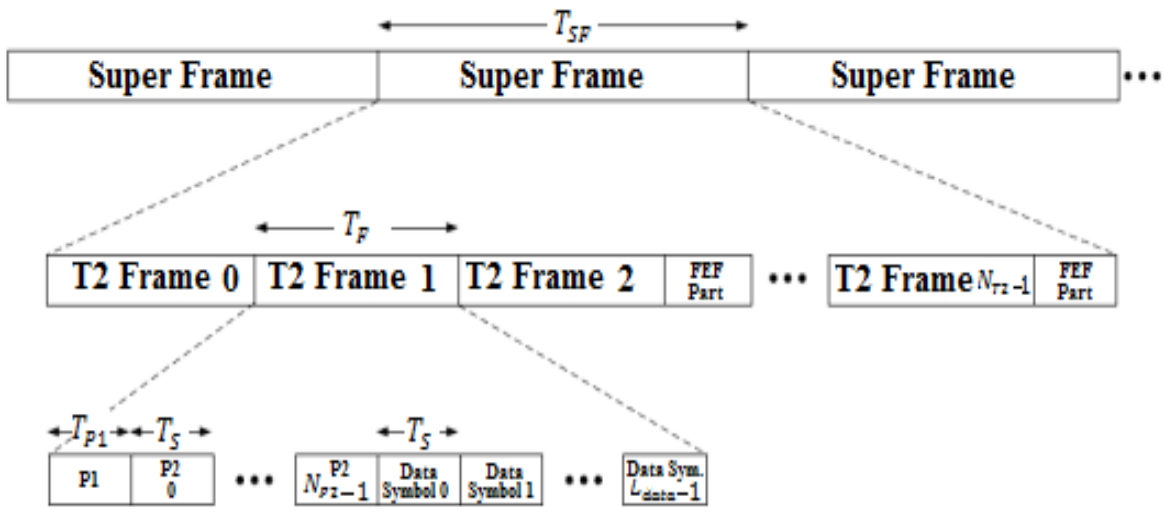

Fig. 5 The DVB-T2 frame structure

The OFDM generation block takes the cells produced by the frame builder, as frequency domain coefficients, and inserts the relevant reference information, known as pilots who allow the receiver to compensate for the distortions introduced by the transmission channel, and to produce from this the basis for the time domain signal for transmission. Pilots also can be used for frame synchronization, frequency synchronization, time synchronization, and channel estimation. The DVB-T2 system uses four types of pilot: scattered pilots, continual pilots, edge pilots, and P2 pilots. The dummy tone reservation block reserves cells of the OFDM for the purpose of PAPR reduction. OFDM systems use different methods to overcome intersymbol interference, which are the guard interval and the cyclic prefix. The DVB-T2 system uses the guard interval method. Finally the data is converted to an analog signal by an DAC (Digital to Analog Converters)[2].

3. Proposed System Implementation

The simulation of the system is done using the Matlab Simulink. Some blocks calls functions from the m-file as these blocks don't exist in the Simulink libraries while others are called as found in Matlab Simulink library. The implemented transmitter is given in Fig. 5.

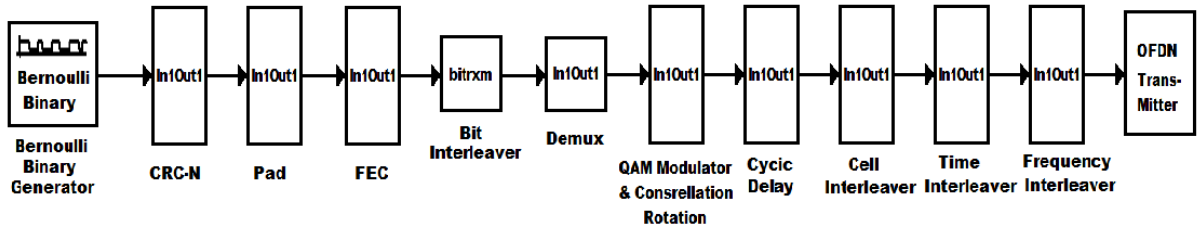

Fig. 6 DVB-T2 implemented transmitter

The first five blocks that represents the input processor is composed of the Bernoulli's Binary, CRC-N, Pad insertion, and scrambler blocks are simulated using ready blocks in the Matlab Simulink. Where the number of samples per frame in the Bernoullis Binary defined as 1504 bits (188 Bytes). The N in the CRC is 8, and the polynomial equation of the Scrambler is .After padding insertion the column size must be 38688. The output of these blocks is a stream of 38688 scrambled bits including the 80 bits for signaling.

The FEC block is the concatenation of the BCH encoder and the LDPC encoder .These two blocks, are simulated using ready blocks in the Matlab Simulink. The chosen values of the two encoders are K_{BCH}=38688, N_{BCH}=38880 and N_{LDPC}= 64800 for the rate 3/5.Where K_{BCH} and N_{BCH} are the BCH encoder message and codeword size. N_{LDPC} is the LDPC encoder codeword size. The input of this block is a stream of 38688 bits and the output is a 64800 encoded bit stream.

An M-file code is written for the bit interleaver. The data coming out of the FEC is divided into information bits and parity bits. The parity bits are then divided into 360 blocks of Qldpc bits, where the value of QLDPC is 72 bits for the considered rate. Then a parity interleaver interleaves these bits by taking the first bit of every block cascaded with the second bit of every block, until the last bit of the last block. The interleaved bits are then rejoined with the information bits and then fed to the column twist interleaver. The column twist interleaver writes the bits column wise (N_c) and reads it row wise (N_r) with a starting position twist t_c at each column. This means that for a given column the writing will start at the row number t_c down to the last row and then will continue at the first row down to the row number t_c-1. [6]

The reading, in the meantime, is simply done from the left to the right. To perform this function we choose the writing position of each block and the rest of the bits are rotated and written in the empty places in the column as shown in Fig.4. The valuesN_c,N_r and t_c are chosen as N_c=12, N_r=5400 andt_c== [0 0 2 2 3 4 4 5 5 7 8 9].

An M-file code is written for the Demux block. The demux is in itself could be considered as a simple interleaver. The input stream is of dimension 64800*1 this stream must be reshaped to a matrix of dimension (5400*12). The parameters of the interleaver are mentioned in [2]. A reshape function is used to return the bits back into a stream (64800) for the next block.

The Rectangular Qam (Quadrature Amplitude Modulation) block is simulated using ready blocks in the Matlab Simulink.The M-ary number for the modulation technique used and the rotation angle for the constellation rotation are chosen to be 64QAM and 8.6 degree.

For the cyclic delay block the cells from the imaginary component of the Qam (Quadrature Amplitude Modulation) stream is multiplied by an angle of 90 degrees (for one cell delay). The output is similar to the input which consists of 10800 cells.

The cell interleaver is simulated using an M-file code. The concept of the cell interleaver is to permutate the output stream of the cyclic delay block. The permutation function is mentioned in [1].For the permutation function $N_d$is chosen to be 14, where N_d is Number of bits in Cell Interleaver sequence. The output stream consists of 10800 bits

A Matlab reshape function is used to simulate the time interleaver, as mentioned before for a single PLP. The number of rows and columns must be specified for each reshape function .The input of the time interleaver block is a stream of 64800 bits while the output is a matrix of dimension functions (2160*5)

The Frequency interleaver is used to map the bits of the time interleaver to the OFDM carriers by a permutation function. It takes the bits from the time interleaver and reshapes it to a stream of dimensions (10800*1), and then it separates these bits into even bits and odd bits. This is done by the Modulus function. After that these bits are permutated as mentioned in [2] considering the IFFT length. The interleaver is simulated using an M-file code. For the permutation function you must define the following parameters N_r , the IFFT length, the numbers of carriers and the numbers of bits in each OFDM symbol . N_r is chosen to be 14 the IFFT length is 16K the number of carriers are 13633. N_r is Number of bits in cell interleaver sequence.

The OFDM generation block can be simulated using two different methods either by using ready blocks in Simulink libraries or calling functions from the m-file code. For both ways it is a simple OFDM function as in [8]. The output is an OFDM signal of 8MHZlength.

4. Results

In this section we will intense our work by testing our implemented system for different rates .The rates that are applied other than the rate (3/5) used and discussed in section 3 are rate 2/3 and rate 5/6.These rates are for the same Modulation technique (64Qam) and for the same IFFT length (16K).The output for all the rates is an OFDM signal of Bandwidth 8 MHZ as seen in Fig. 7. The constellation diagram (without rotation) of the modulator (64QAM) is shown in Fig. 8, while the constellation after rotation is shown in Fig. 9.

5. Conclusion

A detailed DVB-T2 transmitter using Matlab is implemented and tested .The implementation is performed using m-files, while the testing is done for different rates (5/6,2/3,3/5).The OFDM output is always 8 MHZ independent on the data rate. In the Ongoing research this transmitter will be redesigned using VHDL design language and will be implemented on a FPGA

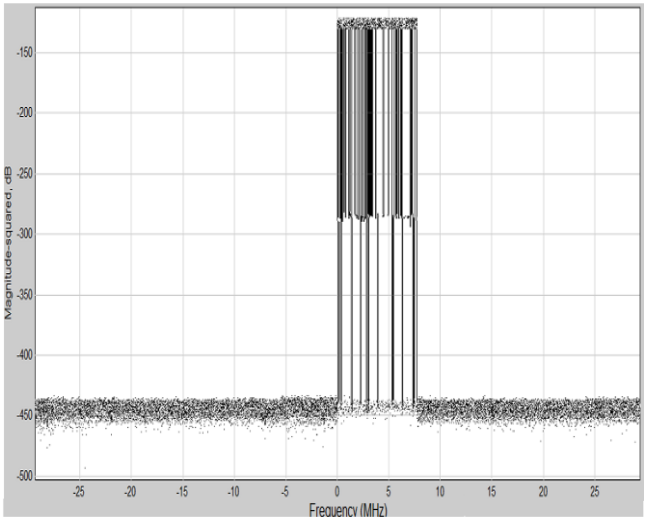

Fig. 7 An OFDM signal of 8 MHZ

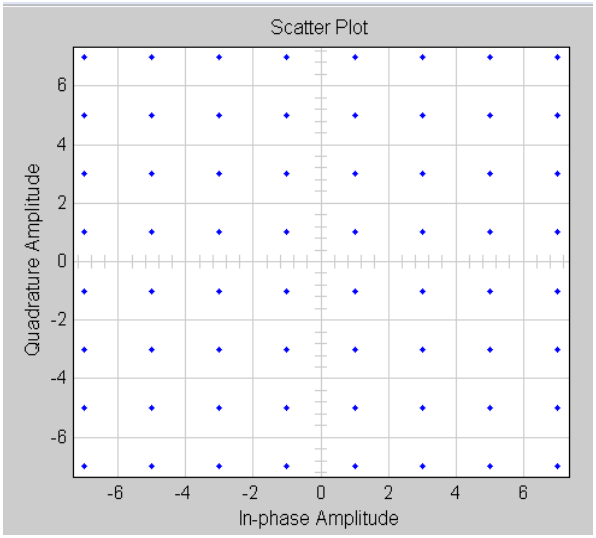

Fig. 8. A 64 QAM constellation mapping without rotation

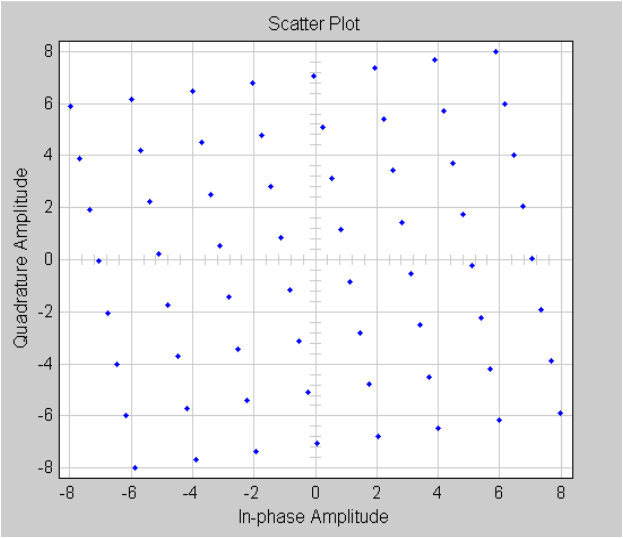

Fig.9 A 64 QAM constellation mapping with rotation.

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