# Reliability prediction of on-board subsystem satellite by Monte Carlo methodology

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# Reliability prediction of on-board subsystem satellite by Monte Carlo methodology

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**Abstract.** This paper presents a case study that aims to develop a hardware design for the pc to the satellite, supported fault-tree design and calculations of dependableness. The on-board pc of a satellite, inserted into the on-board management system, has functions of receiving, process and distribution of commands to the subsystems and payload of the satellite; and exploit, formatting, storage and transmission of measurement from subsystems and payload. The most necessities of associate on-board pc are high dependableness, capability of real time process, resistance to radiation, and minimizing power consumption, volume and mass. Enlarged dependableness is achieved by the fault tolerance technique that relies on adding redundancy to the system, or the utilization of elements with high price of individual dependableness. During this work, hardware redundancy techniques are thought-about. First, a pc is meant and its dependableness is calculated, for a mission of one year period. Mission dependableness goal isn't earned during this calculation. So as to extend dependableness, two kinds of fault tolerant redundant architectures are analyzed, with their various reliabilities calculated for the identical amount of the mission.

**Keywords**: Reliability; Fault-tree; On-board computer (OBC); Redundancy; Satellite; Monte Carlo Methodology

## 1. Introduction

A satellite, within the system vision, will be divided into: Structure, Power provide, Orbit and angle management, Propulsion, Communication Service, On-Board Management, Thermal management and Payload [1]. A satellite is AN isolated system that's onerous to succeed in with a very restricted communication system once it's launched. If the satellite fails, it's terribly troublesome to repair it. Thus, the satellite should work well throughout its time period despite exposure to a fault prone surroundings. There are several threats to a satellite such as area environments, network issues, and software package faults, etc.

Generally, the satellite operates for a really long period. The satellite is exposed to harsh environment; there are several environmental threats like star nucleon effects and electrons harm caused by cosmic rays. They cause spurious commands and incorrect knowledge [2]. Network threats conjointly exist. The satellite will be exposed to wrong commands caused by spoofing of uplinks and viruses [3].

Reliability is outlined because the chance of a system or a subcomponent functioning properly underneath bound conditions over an interval of your time [4]. As an example, the dependableness of network nodes, termed because the terminal dependableness, is that the chance that a collection of operational edges provides communication ways between each try of nodes [5].

The On-Board computer, inserted into the system of On-Board Management, could be an important purpose for the satellite. Its functions such as: reception, process and distribution of commands to the subsystems and to the payload; and acquisition, formatting, storage and transmission of measurement to the system and to the payload. Main needs of associate degree on-board laptop are: high responsibility, capability of real time process, resistance to radiation, low power consumption, and physically reduced mass and volume. Responsibility is vital for the house mission success, by reason of the high prices of maintenance if it's potential. To achieve high responsibility primarily will be invested with in two action lines: use of individual parts with high responsibility, or application of fault tolerance technique, that consists of adding redundancy to the system. Redundancy could also be gift in hardware system, software, time or data. Selections on once and the way to design-in redundancy rely upon the criticality of the system or operate and should be balanced against the necessity to reduce complexness and price. It's usually potential to produce worthy responsibility enhancements by mistreatment redundant circuit components, at comparatively very little price, due to the low price of newest devices [6].

The Fault Tree (FT) is a well-known method that efficiently analyses the failure causes of a system and serves for reliability and availability evaluations [7]. Using popular, simple and standard notation, the Fault Tree (FT) [8] method provides an ideal framework for deductive analyses of causal relationships between a system fault and associated failure events. It also allows the calculation of probabilities related to the combinatorial logic of several associated gates. Therefore, it is suitable for both qualitative, quantitative analyses and is widely used in reliability and safety studies.

The Monte Carlo methodology could be a technique that may be wont to solve mathematical or applied math issues. Monte Carlo simulation uses frequent sampling to see the properties of some development. There are terribly rare uses of such simulation strategies for code testing [9].Monte Carlo ways may also be accustomed calculate the system responsibility. Most techniques are designed for continuous-time models [10, 11] or qualitative analysis [12], however adaptation to single-time models is straight forward. Every part is willy-nilly appointed a failure state supported its failure chance. The linear unit is then evaluated to work out whether or not the FT has failing. Given enough simulations, the fraction of simulations that will not result in failure is some the responsibility.

The present paper, developed a failure percentage model which used to detect the critical elements effects on OBC subsystem, then implementing the redundant technique on the critical components to improve the subsystem predicted reliability by using Monte Carlo simulation with Matlab software.

## 2. Satellite on-board computer (OBC) configuration

The main responsibility of the OBC is to monitor the health of the system and to take necessary actions when situations demand for it. It monitors the health of the satellite by periodically requesting health packages from software instances as well as polling sensors for the different modules' power consumption. It also monitors the satellite battery power level, and sets the satellite state appropriately. In addition to this the OBC also acts as a gateway between the satellite bus, and the radio link to ground station. The satellite is designed as a distributed system with redundant functionalities implemented in different modules. The OBC block diagram shown in figure 1

The satellite architecture requires a standard serial data bus protocol to be used for fast data rate transfers between subsystems. This data transfer is initialized and monitored by the OBCs' central processing unit CPU. Figure 1 shows that the CPU has a multi interfaces to communicate between OBC and the other subsystems in satellite, Additional supporting hardware components to the CPU are necessary to ensure the OBC runs efficiently. It is recommended for the OBC subsystem to include an overcurrent protection circuitry, a battery backed-up real time clock (RTC) and one or more on-board temperature sensors. The overcurrent protection is needed to monitor the current drawn by the subsystem and disconnect the supply in case of an overcurrent condition. The RTC keeps track of the time and

helps to synchronize onboard operations. The RTC also keeps onboard data synchronized with the ground operations. The on-board sensors are devices that detects and responds to some type of input from the physical environment, e.g. battery voltage, solar cell current, thermal and attitude, etc. The temperature sensors are necessary to monitor the variations in temperature at different points of the satellite which are exposed to the harsh space environment. OBC have a memory chips which are FLASH memory (read-only memory) and RAM memory (read and write operation).

## 3. On-board computer reliability

The reliability block diagram is drawn so that each element or function employed in the item can be identified. Each block of the reliability block diagram represents one element of function contained in the item. The blocks in the diagram follow a logical order, which relate to the sequence of events during the prescribed operation of the item [13].

In the present work, the reliability block diagram was generated for OBC subsystem; the main components and type of connections are shown and described in figure 2. This figure shows OBC components connected as a series connection, and the memory system consists of two parallel lines memory system 1&2, each line contains (RAM or FLASH memory, memory controller, and error detection device).The RAM has "2/3""m of n technique", connection which means that one RAM element failure is acceptable but two element failures lead to a RAM failure. The same technique used for the FLASH memory.

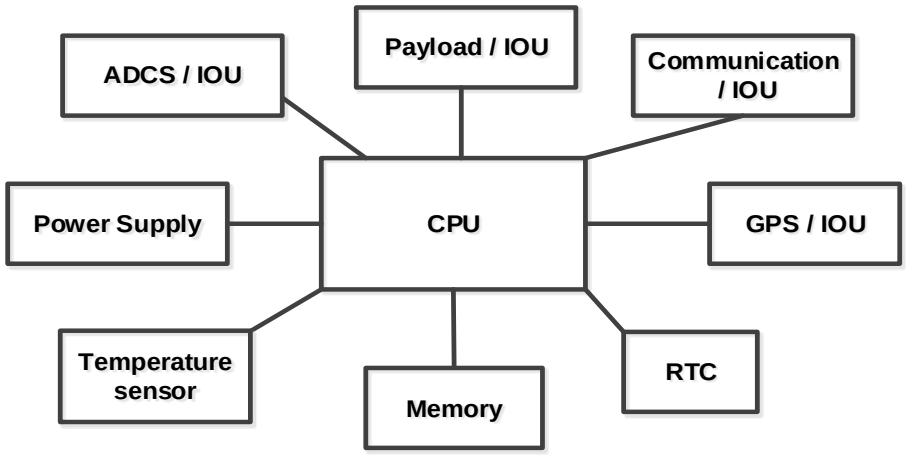


**Fig.1.** Block diagram of the proposed satellite OBC

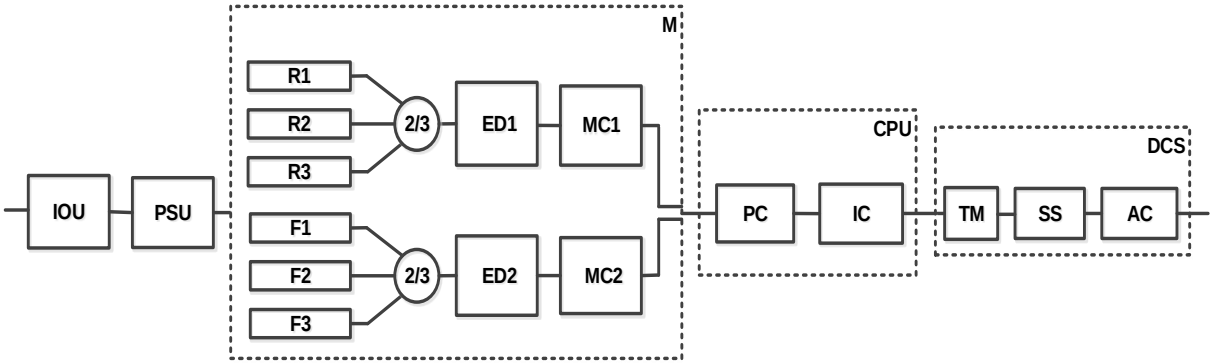


**Fig.2.** On-board computer subsystem (OBC) block diagram

The satellite onboard computer system under study shall provide operation within one year of satellite active lifetime. Reliability data of the on-board computer (OBC) equipment's are presented in Table 1. This table contains the on-board computer subsystem composition, its architecture and components abbreviations. Also, the reliability mathematical model is used to identify weak links, and indicates where reliability improvement activities should be introduced. The OBC subsystem reliability is calculated using reliability values listed in Table 1.1, and is using mathematical reliability equations, for the proposed OBC reliability block diagram presented in the previous Fig.2, reliability of OBC subsystem is calculated to be = 0.947

## 4. Onboard Computer (OBC) Failures

A conventional Probability Modeling Method is used to determine the mathematical model on-board computer. The reliability equations could also be expressed as shown in the following sections:

The reliability $R_I$ (t) of any component at any time t is given by [14]:

$$R_i(t) = e^{-\lambda t} \tag{1}$$

The sum of reliability and probability of failure is equal to one. Using this theorem, the probability of failure of an element can be shown by:

$$F_i(t) = 1 - R_i(t) = 1 - e^{-\lambda t} \tag{2}$$

$$F_s(t) = 1 - R_s(t) \tag{3}$$

where:

**λ**: failure rate

$F_i$ (t): probability of failure for one element (component)

$F_s$(t): probability of failure for system

$F_{sf}$(t): probability of failure for system when one element has a highest reliability

$$F_{sf}(t) = F_s(t) - F_i(t) \tag{4}$$

$$F_{sf}(t) = 1 - \frac{R_s(t)}{R_i(t)} \tag{5}$$

Contributions of any components in satellite failure (Failure %)

$$\text{Failure } \% = \frac{F_s(t) - F_{sf}(t)}{F_s(t)} \times 100 \tag{6}$$

The contribution percentage for each component of onboard computer (OBC) subsystem failures was calculated by using the reliability values in table 1 and equations (5.6). Failures percentages results are shown in table 2:

From table 2 notice that failures% for each RAM (R1, R2, and R3) equals to 7.18% for each one. These percentages reduced to be 0.18% after using k out of n system (a special case of parallel system). The same comparison between failure % results for F1, F2, and F3 with failure % for FLASH memory (using k out of n system). These comparisons results shows that "RAM" memory and "FLASH" memory are absolute reliable under k out of n system.

A comparison between failure % results for the OBC subsystem components implemented as shown in figure 3, this comparison needed to detect the most critical components to be discussed and improved.

**Table 1** Onboard computer (OBC) reliability parameters

| Components | Abb. | Reliability Values |
|---|---|---|
| On-board Computer | OBC | 0.947 |
| In / Out Unit | IOU | 0.994 |
| Power Supply Unit | PSU | 0.987 |
| RAM 1 | R1 | 0.996 |
| RAM 2 | R2 | 0.996 |
| RAM 3 | R3 | 0.996 |
| FLASH 1 | F1 | 0.995 |
| FLASH 2 | F2 | 0.995 |
| FLASH 3 | F3 | 0.995 |
| Error Detection 1 | ED1 | 0.997 |
| Error Detection 2 | ED2 | 0.997 |
| Memory Controller 1 | MC1 | 0.996 |
| Memory Controller 2 | MC2 | 0.996 |
| OBC-Processor | PC | 0.995 |
| Interface Control | IC | 0.991 |
| Timer | TM | 0.995 |
| Sensors | SS | 0.997 |
| Actuators | AC | 0.996 |
| Central Processing Unit | CPU | 0.986 |
| Memory System | M | 0.9999 |
| Memory System 1 | M1 | 0.993 |
| Memory System 2 | M2 | 0.993 |
| Data Control System | DCS | 0.979 |
| Main System | MS | - |
| Software | SW | - |

**Table 2** Failures % for OBC subsystem components

| No. | Component | Failures % |
|---|---|---|
| 1 | IOU | 10.8% |
| 2 | PSU | 23.5% |
| 3 | R1,R2,R3 | 7.18% |
| 4 | RAM | 0. 18% |
| 5 | F1,F2.F3 | 8.98% |
| 6 | FLASH | 0.18% |
| 7 | ED | 5.38% |
| 8 | MC | 7.18% |
| 9 | PC | 8.98% |
| 10 | IC | 16.2% |
| 11 | TM | 8.98% |
| 12 | SS | 5.38% |
| 13 | AC | 7.18% |

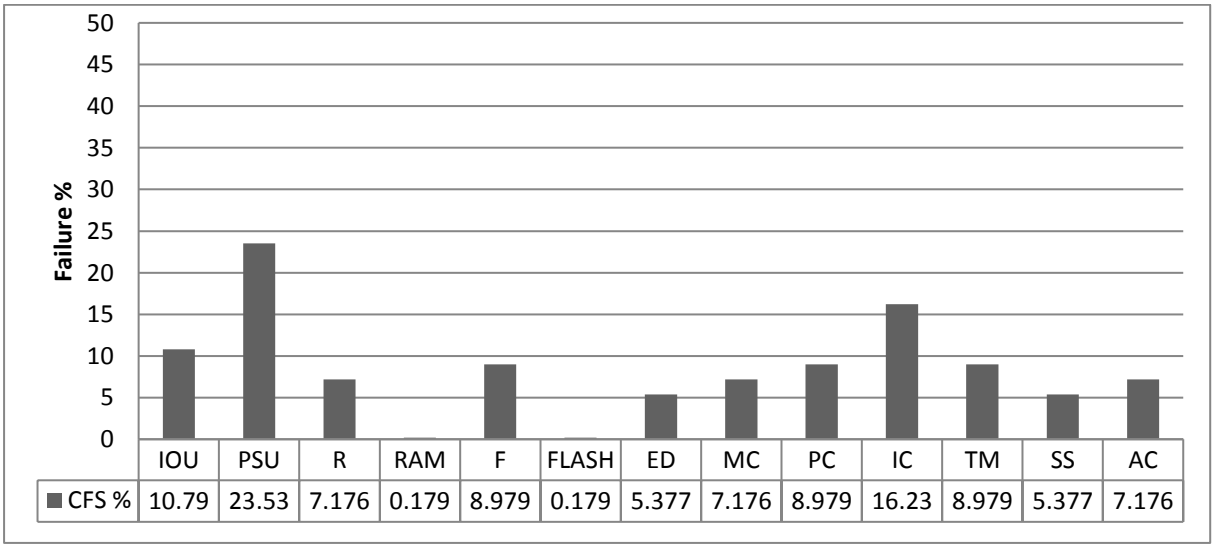


**Fig.3** (Failure %) for OBC subsystem components

Results presented in Fig. 3 illustrate clear identification of the most probable component affecting system failure. The PSU & IC columns are the most critical elements in the system, which leads to OBC system failure so it is the candidate elements to be redundant.

Applying redundant for PSU with $PSU_T$ as parallel set, and IC with $IC_T$ as parallel set, Evaluations of system reliability and recalculation of failure contribution percentage factors for these components are shown as follows:

Backup technique is used to increasing reliability of the system by including a backup or identical component, to the system that will take over if the original component fails. This backup technique is known as redundancy. Redundancy is not a solution to all reliability problems since redundant systems usually increase weight, cost, and complexity, but redundancy is a good solution for backing up inherently unreliable components that are essential to the success of the system [15]. Parallel redundant "Cold standby" technique is used on PSU & IC components to increase reliability. The reliability block diagram of the "cold standby" is shown in Fig. 4.

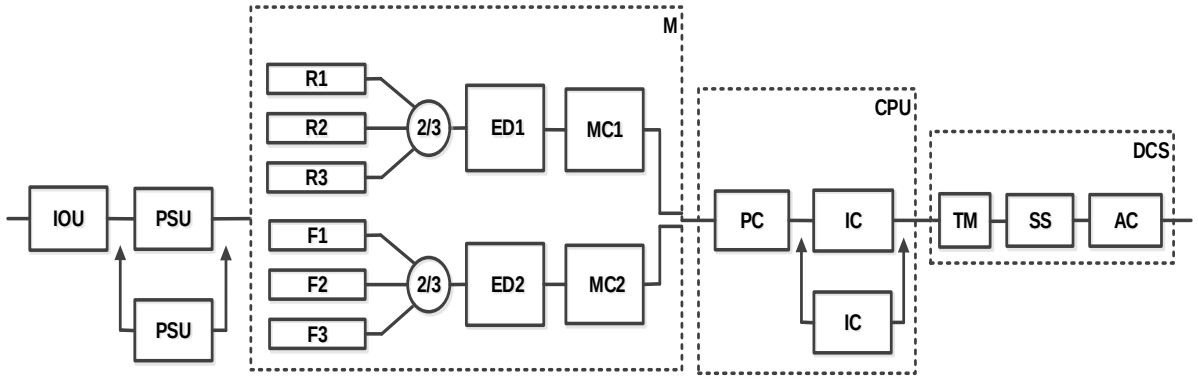


**Fig.4.** On-board computer subsystem (OBC) block diagram with cold standby

**Table.3** Critical components using cold standby

| Components | $PSU_T$ | $IC_T$ |
|---|---|---|
| Reliability | 0.998 | 0.999 |
| Failure % | 0.137 % | 0.12% |

Recalculations for OBC reliability using "PSU"& "IC" cold standby data from table 3, the results indicate that backup technique improve OBC reliability to be 97% instead of 94.7%

## 5. Fault Tree

The fault tree analysis (FTA) is a deductive procedure used to determine the various combinations of hardware and software failures and human errors that could cause undesired events (referred to as top events) at the system level. The deductive analysis begins with a general conclusion, then attempts to determine the specific causes of the conclusion by constructing a logic diagram called a fault tree. The basic symbols used in an FTA logic diagram are called logic gates which are similar to the symbols used by electronic circuit designers [16]. The proposed satellite onboard computer has been analyzed and its fault tree is presented clearly in figure 5.

## 6. Reliability Prediction

Applicable subsystem satellite onboard computer (OBC) configurations are introduced and a reliability and failure rate specifications applied as shown in table 4. Conventional and advanced reliability modeling applied for estimation and analysis of OBC reliability. The satellite OBC reliability prediction was based on the advanced Monte Carlo Simulation technique using MATLAB software (R2018a). MATLAB program generates the prediction reliability values over one year (8760 hr.) of OBC lifetime, by using the total failure rate value (9.85E-06) exists in table 4 the prediction reliability equals to 86% as shown in Fig.6, this result detected without using any redundant for OBC components.

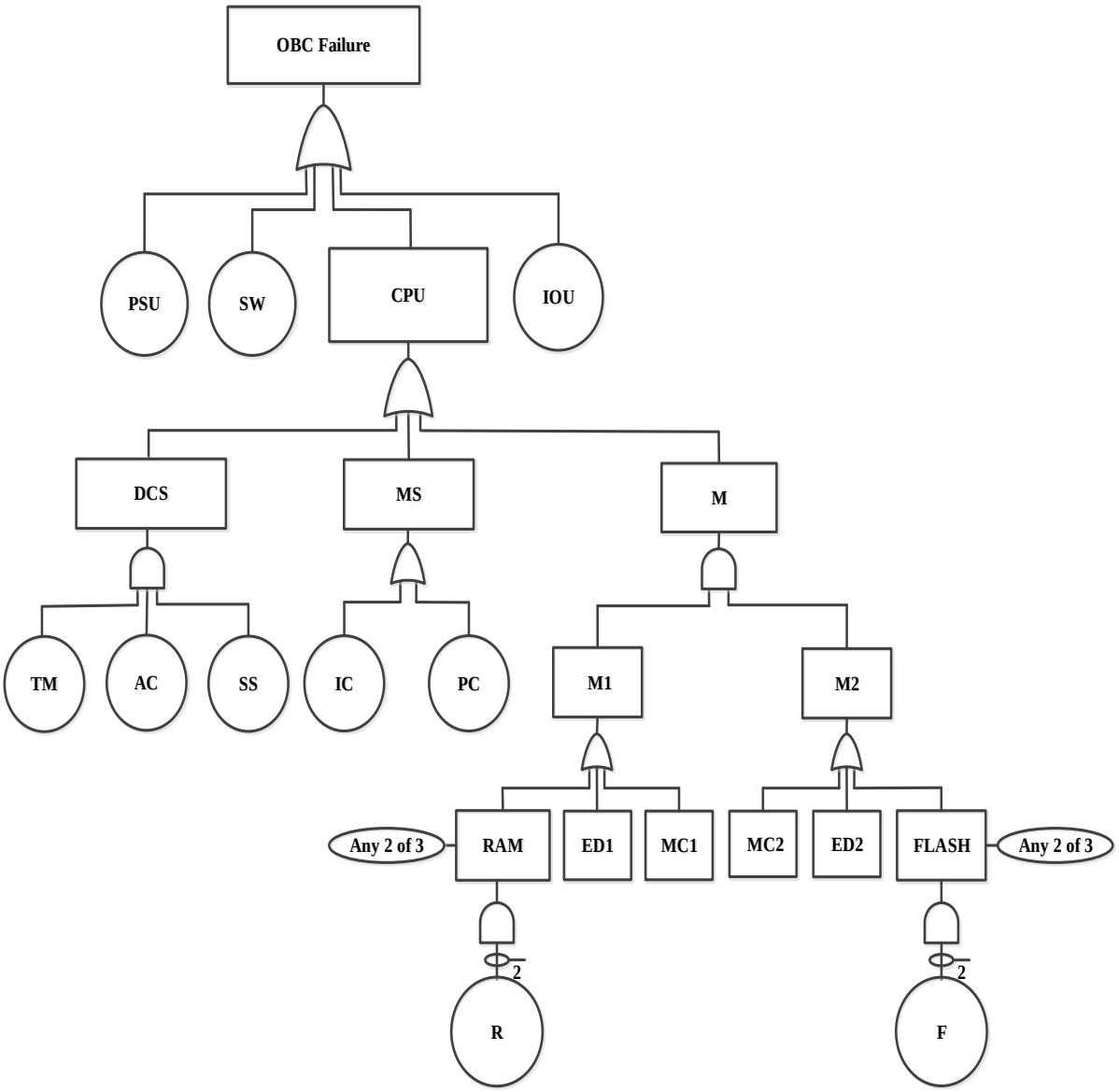


**Fig. 5.** Fault Tree for the proposed on-board computer

**Table 4** Failure rate values for OBC components (before improvement)

| No. | Components | R | λ |
|---|---|---|---|
| 1 | IOU | 0.994 | 6.86995E-07 |
| 2 | PSU | 0.987 | 1.49375E-06 |
| 3 | R1 | 0.993 | 4.57537E-07 |
| 4 | R2 | 0.993 | 4.57537E-07 |
| 5 | R3 | 0.993 | 4.57537E-07 |
| 6 | F1 | 0.994 | 5.72208E-07 |
| 7 | F2 | 0.994 | 5.72208E-07 |
| 8 | F3 | 0.994 | 5.72208E-07 |
| 9 | ED1 | 0.997 | 3.4298E-07 |
| 10 | ED2 | 0.997 | 3.4298E-07 |
| 11 | MC1 | 0.996 | 4.57537E-07 |
| 12 | MC2 | 0.996 | 4.57537E-07 |
| 13 | PC | 0.995 | 5.72208E-07 |
| 14 | IC | 0.991 | 1.03205E-06 |
| 15 | TM | 0.995 | 5.72208E-07 |
| 16 | SS | 0.997 | 3.4298E-07 |
| 17 | AC | 0.996 | 4.57537E-07 |
| Before Redundant | | | 9.85E-06 |

**Table 5** Failure rate values for OBC components (after using memory redundant)

| No. | Components | R | λ |
|---|---|---|---|
| 1 | IOU | 0.994 | 6.86995E-07 |
| 2 | PSU | 0.987 | 1.49375E-06 |
| 3 | * RAM | 0.999 | 1.14161E-08 |
| 4 | * FLASH | 0.999 | 1.14161E-08 |
| 5 | ED1 | 0.997 | 3.4298E-07 |
| 6 | ED2 | 0.997 | 3.4298E-07 |
| 7 | MC1 | 0.996 | 4.57537E-07 |
| 8 | MC2 | 0.996 | 4.57537E-07 |
| 9 | PCT | 0.995 | 1.14161E-08 |
| 10 | IC | 0.991 | 1.03205E-06 |
| 11 | TM | 0.995 | 5.72208E-07 |
| 12 | SS | 0.997 | 3.4298E-07 |
| 13 | AC | 0.996 | 4.57537E-07 |
| Using memory chips redundant | | | 6.78E-06 |

Table 5 shows failure rate value for OBC subsystem after using memory redundant, then study and analyze the effect of the new redundant configuration for memory chips component using MATLAB software. Reliability prediction is increased to 93 % as shown in Fig.7. Through the failure rate and life expectancy of one year (8760 hr.) from table 6, the on-board computer failure rate with cold standby redundancy for PSU & IC & and memory chips components is equal to 4.28E-06; using this improved value with MATLAB software to have the reliability prediction percentage after the final improvement. Notice that reliability prediction percentage increased to 96% as shown in Fig.8

From all the above results we find that reliability prediction percentage improved with 11 % after using the redundant technique for (PSU, Memory chips and IC) components, and using redundant technique for a separate components in OBC subsystem improve the reliability percentage without duplicate the whole subsystem which reduced the total cost .

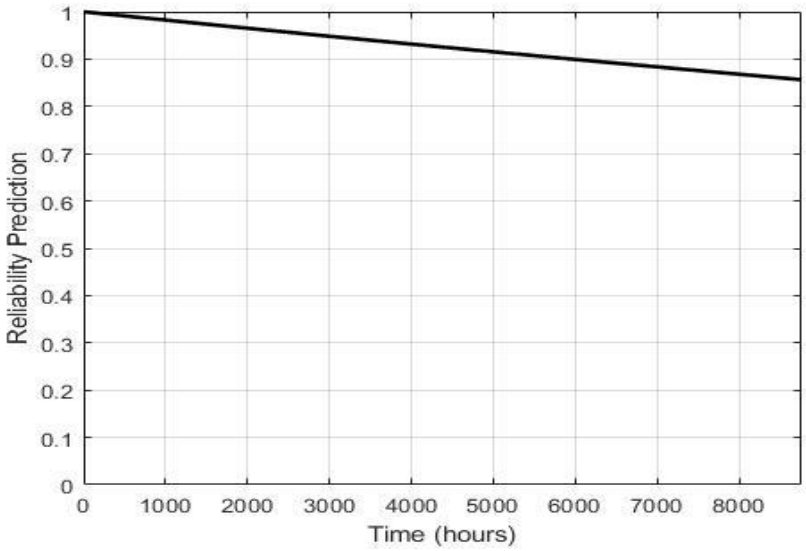


**Fig.6** Reliability prediction over one year of OBC lifetime is equal to 86% (Without redundant)

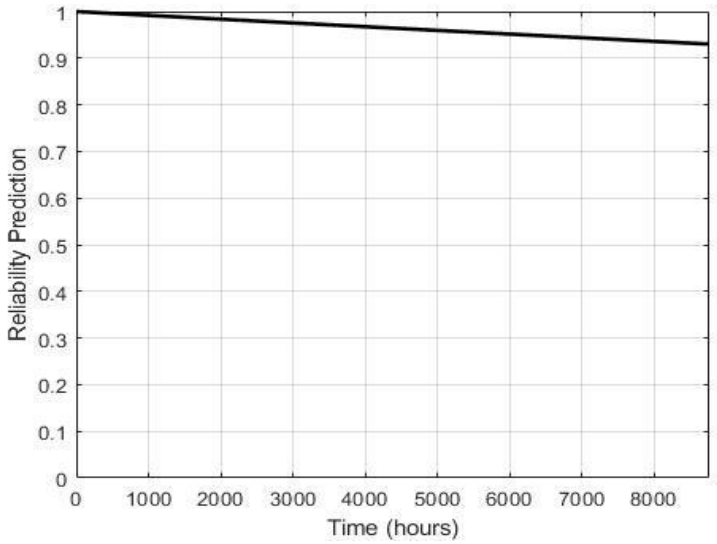


**Fig.7** Reliability prediction over one year of OBC lifetime is equal to 93% (Using memory redundant)

**Table 6** Failure rate values for OBC components
(* after improvements)

| **No.** | **Components** | **R** | **λ** |
|---|---|---|---|
| 1 | IOU | 0.994 | 6.86995E-07 |
| 2 | * PSUT | 0.999 | 1.14161E-08 |
| 3 | * RAM | 0.999 | 1.14161E-08 |
| 4 | * FLASH | 0.999 | 1.14161E-08 |
| 5 | ED1 | 0.997 | 3.4298E-07 |
| 6 | ED2 | 0.997 | 3.4298E-07 |
| 7 | MC1 | 0.996 | 4.57537E-07 |
| 8 | MC2 | 0.996 | 4.57537E-07 |
| 9 | PCT | 0.995 | 1.14161E-08 |
| 10 | * IC | 0.999 | 1.14161E-08 |
| 11 | TM | 0.995 | 5.72208E-07 |
| 12 | SS | 0.997 | 3.4298E-07 |
| 13 | AC | 0.996 | 4.57537E-07 |
| After Redundant | | | 4.28E-06 |

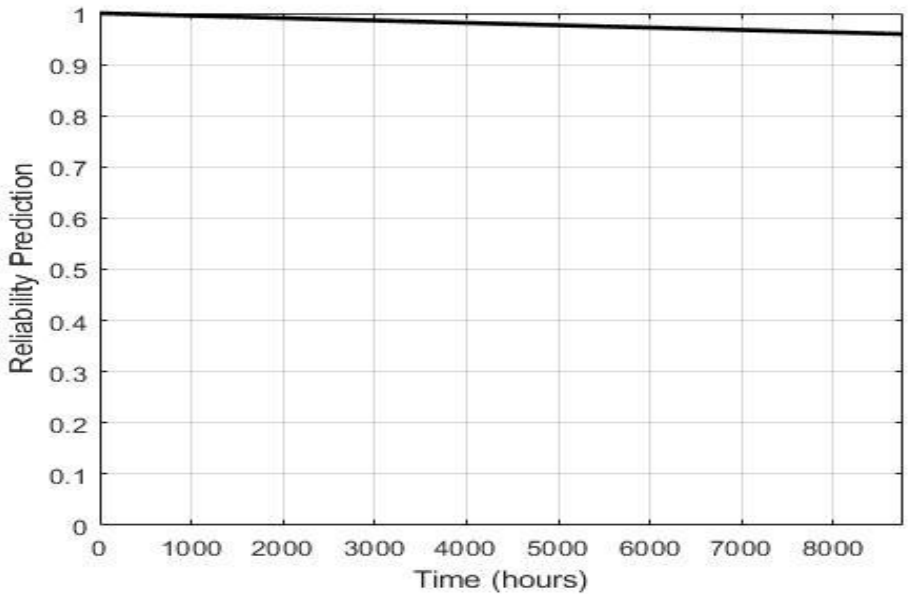


**Fig.8** Reliability prediction over one year of OBC lifetime is equal to 96% (After redundant)

## 7. Conclusion

The reliability modeling results from the application of Monte Carlo simulation technique is more effectiveness to predicate on the dynamic fault tree of the orbit satellite system. The established mathematical models based on Monte Carlo simulation of the modeling the reliability of satellite on-board computer subsystem have been to quite unique, powerful and flexible. These models reflect the complex, interactive and higher order effects of the various input parameters. Predicted reliability improved with 11 % after using the redundant technique for (PSU, Memory chips and IC) components. Using redundant technique for a separate components in OBC subsystem improve the reliability percentage without duplicate the whole subsystem which reduced the total cost .

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